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Designing of Testable Reversible QCA Circuits Using a New Reversible MUX 2×1

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Abstract

Recently testing of Quantum-dot Cellular Automata (QCA) Circuits has attracted a lot of attention. In this paper, QCA is investigated for testable implementations of reversible logic. To amplify testability in Reversible QCA circuits, a test method regarding to Built In Self Test technique is developed for detecting all simulated defects. A new Reversible QCA MUX 2×1 design is proposed for the test layer implementation regarding to overhead and power savings. Our proposed Reversible QCA MUX 2×1 design resulted in decrease in QCA cell counts and minimal input to output delay. The proposed design is simulated and verified using QCA Designer ver.2.0.3.

Keywords: *QCA, Reversible, Fault, MUX, Testability*

1. Introduction

Nano technology has been the focus of extensive research in the recent years. One of the most important difficulties in the development of the modern computational systems is power dissipation of the circuits [1]. A possible solution is reversible computing. Reversible computing considers the relation between information dissipation, which caused energy dissipation, and logical computing, which leads to the thermodynamic limit of computation [25]. Reversible computation is achieved at a logical level by establishing a one-to-one mapping between the input and output vectors in the circuit [2]. The one-to-one mapping is named *bijective* property. For the first time, Landauer investigated the *bijective* property and proved that the lower bound of heat dissipation for losing any bit of information is kTln2 joules, where k is Boltzmann's constant and T is the temperature at which computation is performed. However, if the computation is performed without losing any information, energy dissipation can be avoided [2].

Although, the CMOS technology has provided some significant achievements such as high density, high speed and low power consumption for VLSI systems, the systems are accompanied by many problems. Some of these problems are high leakage current, high power density levels, and extremely high lithography costs [17]. Some believe that these issues will result in the conclusion of the CMOS revolution in the next years [3]. One of the alternatives for CMOS technology is Quantum-dot Cellular Automata (QCA) in which the configuration of an electron pair within a quantum-dot cell

specifies the logical states. In the conventional CMOS circuits, information is transferred using electrical current; whereas, in the QCA circuits, information is transferred by propagation of a polarization state [5]. The QCA circuits potentially have small feature size and ultra-low power consumption. It is believed that a QCA cell of a few nanometers could be constructed through molecular implementation by a self-assembly process [4]. As a result, it is expected that QCA achieves densities of 10^{12} devices/cm^2 and operates at Tera Hertz frequencies [6].

In this paper, QCA is investigated for testable implementations of reversible logic. A test method referenced as Built In Self Test (BIST) technique is implemented for detecting defects in reversible QCA circuits using MUXs 2×1. A process of providing an exhaustive test set is investigated. A new Reversible 2×1 QCA MUX design is proposed which is more efficient and less complex than previously reported designs.

2. Basic QCA Devices

For constructing all components of a QCA circuit including logical gates and also interconnections and wires, a single device is used. This device is a QCA cell which is a set of four quantum dots located at the corners of the cell and an electron pair [18]. By providing tunneling junctions with potential barriers, which are raised to prevent electron movement and lowered to permit electron movement, three states can occur.

When barriers are low, the electrons can localize on any dot and the Null state occurs and when the barrier is raised, the cell is polarized and the other two states can occur. These two states are shown as P = +1 and P = −1 in Fig 1(a), which represent the logic "1" and "0", respectively. Because of coulombic interactions, cells which are located near each other are forced into matching polarizations. The propagation of polarization provides information transfer. In QCA technology, the fundamental logic gate is the Majority Gate or Voter (MV). A majority gate has three inputs and the output is equal to whichever two inputs agree as shown in Fig 1(c). The logic function of majority gate is [16]:

$$M(A, B, C) = AB+BC+CA \quad (1)$$

Logical AND and OR functions can be implemented by setting one input of the MV to "0" and "1", respectively. The inverter is the other basic gate in QCA and is shown in Figure 1b. The binary wire and inverter chain are shown in Figs. 1d, e [18].

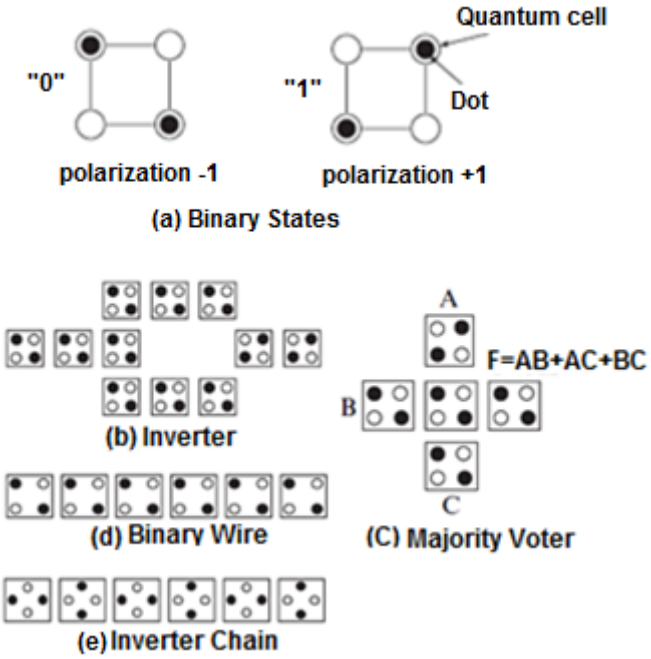

Figure 1. QCA Cell and Basic QCA Devices

2.1 Clocking in QCA

In VLSI circuits, timing is controlled by a reference signal which is called *clock* but timing in QCA is performed by clocking in four periodic phases such as Relax, Switch, Hold, and Release [4]. During the Relax phase, the QCA cell is unpolarized. During the Switch phase, the barriers are raised and a distinctive polarity is obtained. Cells in this phase are affected by the polarization of their neighbors. Actual computation occurs in this phase. During the Hold phase, barriers are high and the cell retains the polarity. In the Release phase, barriers are lowered and the cell loses the polarity. A signal is latched and stays latched until the cells of the next clocking zone switches to the Hold phase and act as input to the subsequent zone. This clocking mechanism allows inherent pipelining [10-11] and obtains multi-bit information transfer for QCA implementation [18].

Landauer clocking scheme is usually used in the QCA implementations. Although, Landauer clocking is simple, it causes power dissipation at some of the QCA circuits shuch as MV. In [8-9], *Bennett clocking* scheme has been proposed for QCA implementations which using it makes MV non-dissipative. Bennett clocking scheme is based on this principle that the bit information is held in place until the current operation is completed [9]. Then, information is erased in the reverse order of computation. It is evident every cell is only switched and released when all other cells are in the same formation, and has a driver of same polarization. Every cell works reversibly. So, the computing process of the whole circuit is reversible. For QCA circuits, quantum-dynamic calculation has shown that energy dissipation per switching event is much less than kTln2 joules of energy [9]. Using Bennett clocking scheme does not require any change in QCA layout, only clocking signals are modified. On the other hand, the control of Bennett clocking is more complex than Landauer clocking scheme and the next operation cannot begin until the circuit is released from the output to the current input, hence, the speed of a computation with Bennett clock is proportional to

the number of clocking zones of the circuit. A cell is released after one clock cycle in Landauer clock, hence, it can participate in the next operation and pipeline is possible. Inherent pipeline in Landauer clock increases the speed of the computations. But Bennett clocking releases the cells from output to input, so the last cell is locked [12]. As a result, there is a tradeoff between reversible computing resulted in no power dissipation and delay when choosing the desired clocking scheme for a QCA implementation.

2.2 Reversible QCA gates

In this section, the QCA implementation of Toffoli and Fredkin gate is presented [13-14]. Two Reversible gates which denoted as QCA1 and QCA2 are also presented [12]. Fredkin, Toffoli, QCA1 and QCA2 gates have three inputs and three outputs and are universal. A QCA implementation of Fredkin, Toffoli, QCA1, and QCA2 gates are shown in Figure 2a, 2b, 2c and 2d, and also three output functions of them are shown in equation 1, 2, 3 and 4, respectively [18]. The Fredkin gate uses a two-level MV implementation with 6 MVs. Toffoli is also a two-level MV implementation with 4 MVs. QCA1 and QCA2 gates require only one-level MV implementation of QCA with 3 MVs. QCA2 has similar properties to QCA1[12].

$$\begin{cases} V = u \\ y_1 = \bar{u}x_2 + ux_1 \\ y_2 = \bar{u}x_1 + ux_2 \end{cases} \quad (1)$$

$$\begin{cases} y_1 = x_1\overline{x_2} + x_1\overline{x_3} + \\ \overline{x_1}\,x_2x_3 \\ y_2 = x_2 \\ y_3 = x_3 \end{cases} \quad (2)$$

$$\begin{cases} y_1 = MV(x_1 + x_2 + x_3) \\ y_2 = MV(x_1 + x_2 + \overline{x_3}) \\ y_3 = MV(\overline{x_1} + x_2 + x_3) \end{cases} \quad (3)$$

$$\begin{cases} y_1 = MV(x_1 + x_2 + x_3) \\ y_2 = MV(x_1 + x_2 + \overline{x_3}) \\ y_3 = MV(\overline{x_1} + x_2 + \overline{x_3}) \end{cases} \quad (4)$$

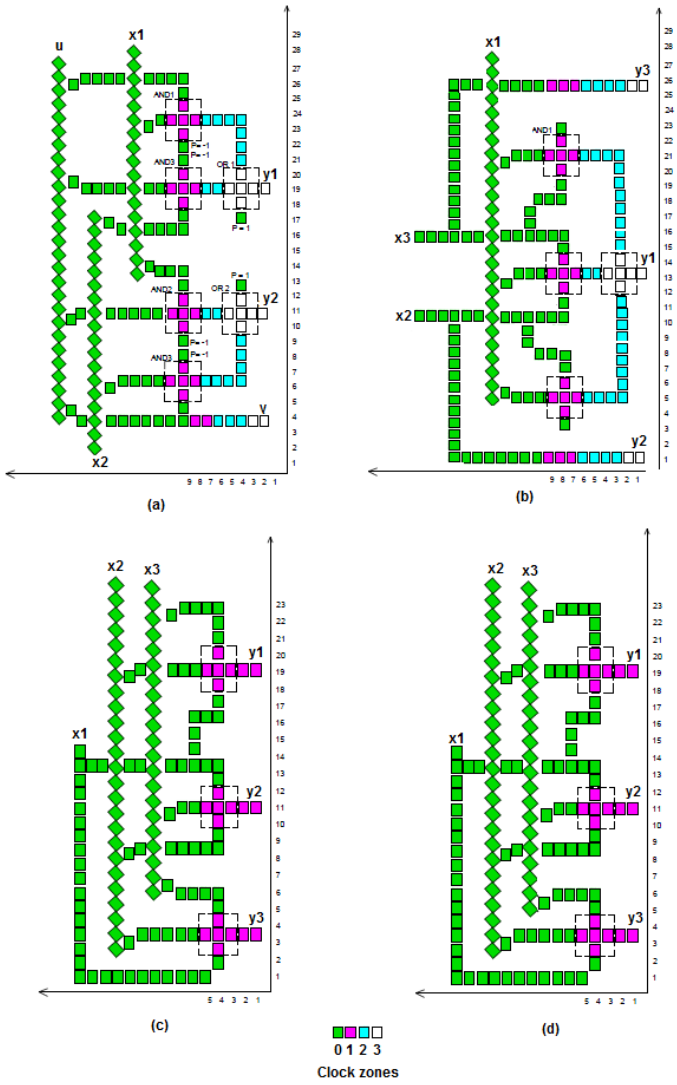

Figure 2. QCA Implementation of Reversible Gates

3. Design and Simulation Results

A test method regarding to BIST is used to increase the testability of Reversible QCA circuits. Complex combinational circuits are usually implemented in several layers in QCA; hence, the test method uses this multi-layer property and is established on circuit partitioning capability. To implement the considered test method, the circuit must be partitioned and divided efficiently as the main inputs and outputs are placed in the main layer and the test inputs and outputs are placed in the test layer. QCA Circuit Partitioning is investigated in [7]. The part of the circuit is more susceptible to defects, is shown as *Unit Under Test* in the Block diagram of Figure 3. When the test control signal is one, the UUT operates in its ordinary condition. However, when the test control signal is zero, the appropriate test vectors are transferred to the Test Input and the test operation is performed. To implement testable Reversible QCA circuit, a test vector set with 100% coverage should be considered and applied to the UUT through MUXs 2×1 [17] Presents a test generation framework for QCA circuits. The stuck-at-fault test set is not guaranteed to detect all defects can occur in QCA circuits [17]. In the

next section, all types of faults are investigated and the process of providing additional test vectors is considered to ensure that all simulated faults are detected in QCA circuits. In addition a single missing/additional cell fault is considered in the defect analysis of the Reversible QCA gates.

If there are m inputs in the UUT, m MUXs 2×1 are implemented in the test layer. The test method is useful for testing complex circuits with many inputs and has potential to increase the capability of controllability and observability of Reversible QCA circuits.

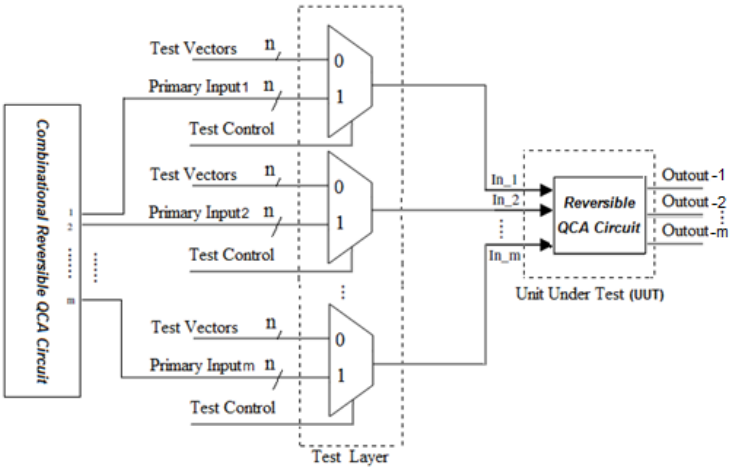

Figure 3. Implementation of the Test Method for a Reversible QCA circuit

3.1 QCA Defects

One of the main challenges for BIST is design of potent test patterns, so that vectors provide satisfactory fault coverage. Because of all defects in QCA aren't covered by the SSF test set, the remained uncovered faults should be simulated and considered. In QCA manufacturing, defects occur in both the *chemical synthesis* phase , which cells are manufactured, and the *deposition* phase, which cells are attached to the substrate, but they are more likely to occur in the deposition phase. If defects occur in the deposition phase, perfect QCA cells are imperfectly placed in the substrate [25].

Defects that are likely to occur in the manufacturing of QCA are illustrated in Figure 4. They are categorized as follows [17]:

1) In a cell displacement defect, the cell is moved from its real place. The defect is shown in Figure 4a.

2) In a cell misalignment defect as shown in Figure 4b, the direction of the defective cell is not correctly aligned.

3) Bridging fault occurs when two interconnections are close or pass over each other, whereupon, the dominant wire determines the output of the dominated wire. There are many possible scenarios that may occur in the presence of a bridging fault and some of them are illustrated in Figure 4c,d. If the displacement distance is denoted as Δnm, the occurred scenario will depend on Δnm and the numbers of displaced cells. It is unknown the defective cells are on which wire and also Δnm is not known, hence, with the assumption that layout information is not available, the number of $n(n-1)$ faults can occur and $2n(n-1)$ conditions must be considered in a QCA implementation with n interconnections. However, more than 50% of these conditions will already be covered by an exhaustive SSF test [17].

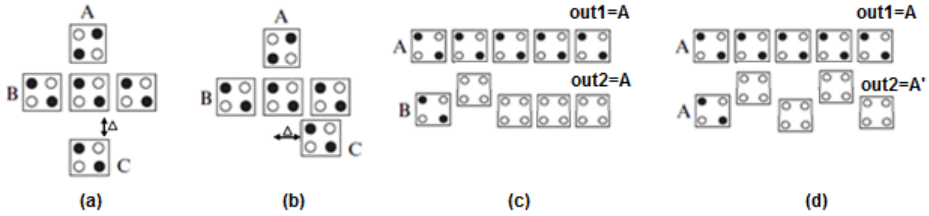

Figure 4. (a) Displacement defect, (b) misalignment defect, (c) - (d) binary wires with a bridging fault[17].

A majority gate has nine possible minimal SSF test sets as shown in Figure 5 that some of them do not cover all simulated faults in the Majority.

SSF_S	100% Defect Coverage?	SSF_S	100% Defect Coverage?
001, 010, 011, 101	√	010, 100, 101, 110	√
001, 011, 100, 101	√	001, 011, 100, 110	× 5 uncovered detect
001, 010, 101, 110	× 1 uncovered detect	010, 011, 100, 101	× 3 uncovered detect
001, 100, 101, 110	√	001, 010, 011, 110	√
		010, 011, 100, 110	√

Figure 5. Minimal SSF test sets for a majority gate.

4) In a missing/additional cell defect, a cell fails to attach to the substrate or additionally is attached to the substrate [12].

[12] investigated a single missing/additional cell in the four Reversible QCA gates and the results for Fredkin, Toffoli, QCA1 and QCA2 gates are shown in Table 1, Table 2, Table 3 and Table 4, respectively, which ai represents the 3 bit pattern whose decimal value is (e.g. a6 = 110), and the ith faulty input-output mapping is shown as fault pattern FPi. The results are obtained by simulating all possible cases and an exhaustive test set consisting of eight input test patterns is used by QCA Designer. The results show that some faults result in the same fault pattern [12].

Table. 1. Fault Patterns of Fredkin Gate

Input Vector	Fault Free	FP 1	FP 2	FP 3	FP 4	FP 5	FP 6	FP 7	FP 8	FP 9	FP 10	FP 11	FP 12	FP 13	FP 14
a0	a0	a0	a1	a1	a0	a1	a0	a1	a2	a2	a0	a0	a2	a2	a0
a1	a2	a3	a3	a3	a2	a3	a3	a3	a2	a2	a3	a2	a2	a0	a2
a2	a1	a1	a1	a1	a1	a1	a0	a0	a3	a3	a1	a1	a3	a3	a3
a3	a3	a3	a3	a3	a3	a3	a2	a2	a3	a3	a3	a3	a3	a1	a3
a4	a4	a4	a5	a4	a4	a5	a4	a4	a4	a6	a4	a4	a6	a4	a4
a5	a5	a5	a5	a5	a4	a4	a5	a5	a5	a7	a5	a5	a7	a5	a5
a6	a6	a6	a7	a6	a6	a7	a6	a6	a6	a6	a6	a4	a4	a6	a4
a7	a7	a7	a7	a7	a6	a6	a7	a7	a7	a7	a7	a5	a5	a7	a5

Table. 2. Fault Patterns of Toffoli Gate

Input Vector	Fault Free	FP 1	FP 2	FP 3	FP 4	FP 5	FP 6	FP 7	FP 8	FP 9	FP 10	FP 11	FP 12	FP 13
a0	a0	a0	a4	a0	a4	a0	a0	a0	a4	a0	a4	a0	a4	a0
a1	a1	a1	a5	a1	a1	a1	a1	a1	a5	a1	a5	a5	a1	a1
a2	a2	a2	a6	a2	a2	a2	a2	a2	a6	a2	a6	a2	a6	a2
a3	a7	a7	a7	a3	a3	a7	a7	a3	a7	a3	a7	a3	a3	a7
a4	a4	a4	a4	a4	a4	a0	a0	a0	a0	a0	a0	a4	a4	a0
a5	a5	a5	a5	a5	a5	a5	a1	a1	a5	a1	a4	a5	a1	a5
a6	a6	a6	a7	a6	a6	a6	a6	a6	a2	a6	a6	a2	a6	a2
a7	a3	a7	a6	a3	a3	a7	a3	a3	a7	a7	a7	a3	a3	a7

Table. 3. Fault Patterns of QCA1 Gate

Input Vector	Fault Free	FP1	FP2	FP3	FP4	FP5	FP6	FP7
a0	a0	a0	a0	a0	a0	a0	a0	a4
a1	a1	a0	a0	a1	a1	a3	a1	a1
a2	a3	a3	a3	a3	a1	a3	a7	a7
a3	a5	a5	a4	a7	a5	a7	a5	a5
a4	a2	a2	a3	a0	a2	a0	a2	a2
a5	a4	a4	a4	a4	a6	a4	a0	a0
a6	a6	a7	a7	a6	a6	a4	a6	a6
a7	a7	a7	a7	a7	a7	a7	a7	a3

Table. 4. Fault Patterns of QCA2 Gate

Input Vector	Fault Free	FP1	FP2	FP3	FP4	FP5	FP6	FP7
a0	a1	a0	a0	a1	a1	a1	a1	a5
a1	a0	a0	a0	a0	a0	a2	a0	a0
a2	a3	a3	a2	a3	a1	a3	a7	a7
a3	a5	a5	a5	a7	a5	a7	a5	a5
a4	a2	a2	a2	a0	a2	a0	a2	a2
a5	a4	a4	a5	a4	a6	a4	a0	a0
a6	a7	a7	a7	a7	a7	a5	a7	a7
a7	a6	a7	a7	a6	a6	a6	a6	a2

The minimal test set for detecting a single missing/additional cell defect with 100% coverage is obtained from the simulation results for each reversible gate. In the presence of weak polarized outputs, signals are restored by QCA lines in the next clocking zone [18]. The minimal test sets are as follow [18]:

– Fredkin gate, the test set has a cardinality of three: vy1y2 = a1 = 001; vy1y2 = a2 = 010 and vy1y2 = a7 = 111.

– Toffoli gate, the test set consists of three vectors: x1x2x3 = a3 = 011, x1x2x3 = a4 = 100 and x1x2x3 = a7 = 111.

– QCA1. The test set consists of three vectors: x1x2x3 = a1 = 001, x1x2x3 = a3 = 011, x1x2x3 = a5 = 101

– QCA2. The test set consists of three vectors: x1x2x3 = a0 = 000, x1x2x3 = a2 = 010, x1x2x3 = a4 = 100.

As a result, the SSF test set that detects every SSF in the circuit is not guaranteed to detect all the simulated QCA defects. For providing an exhaustive test set that defects

all types of defects with 100% coverage, cell displacement, cell misalignment, bridging and single missing/additional cell faults must be simulated by QCA Designer to get associated test vectors then must be added to the SSF test set.

3.2 Designing of MUXs in the Test Layer

It is shown that binary wires can tolerate defects more than inverter chains. Inverter chains are usually used to implement wire crossings in the same layers. For crossing wires, the wire which is along the horizontal or vertical direction is a binary wire, and the other wire is an inverter chain which is located in the perpendicular direction.

But circuits with coplanar wire crossings are more likely to fail [19], hence, a multilayer wire crossover scheme is used to decrease failure rate in QCA circuits.

The vertical interconnect layer is used to implement the test layer to impose minimal overhead. Circuits which are used in the test layer must be reversible with no power dissipation. To implement reversible multiplexer circuits in the test layer, three designs are proposed and investigated. One is using Fredkin gate as a multiplexer circuit, because the logical function of Fredkin has two switched output which both of them operate as a multiplexer. The other one is using Bennett clocking in classical two-to-one MUX scheme. At the end, a Reversible QCA MUX 2×1 design is proposed. The proposed Reversible MUX 2×1 design resulted in decrease in cell counts and decrease in input to output delay in comparison to previously reported counterpart.

Bennett clocking scheme, which offers a practical realization of reversible computing, results in a longer delay about 4 times more than Landauer clock in a two-to-one MUX layout [12]. The QCA layout of two-to-one MUX [23] is shown in Figure 6. Unfortunately, it was impossible to simulate the circuit with Bennett clocking scheme since available version of QCA Designer is associated with Landauer clocking scheme. Four clocking zones are used in QCA layout of two-to-one MUX. If assume m=3 then Applying 3 two-to-one MUXs with occupied rectangular area 14×17 results in the entire layout of 14×57 cells in the test layer.

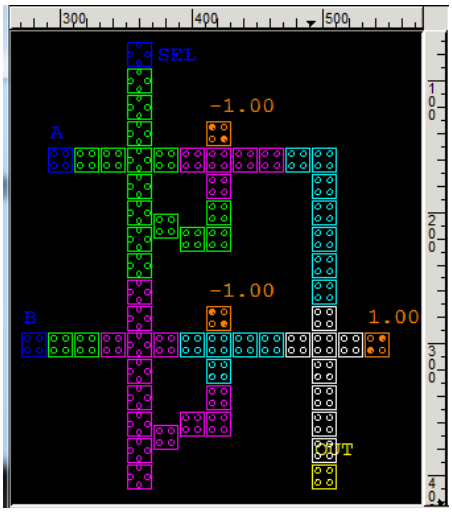

Figure 6. QCA Layout of two-to-one MUX

On the other hand using Fredkin gate, which is a Reversible QCA gate and uses Landauer clocking scheme, makes a QCA system inherently suitable for pipeline computations. It is considerable that Fredkin gate has 6 MVs with occupied rectangular

area two times more than a two-to-one MUX. Hence, it results in input to output delay. Four clocking zones are also used in the QCA implementation of Fredkin gate as shown in Figure 7. Implementation of three Fredkin gates with rectangular area 18×30 results in the entire layout of 18×96 cells.

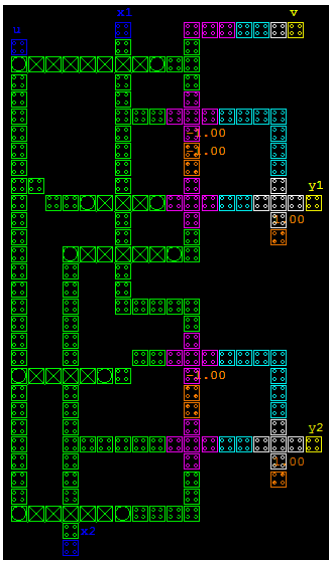

Figure 7. QCA Implementation of Fredkin Gate

3.3 The Proposed MUX 2×1 Design

For the multiplexer circuit to be reversible, the logic function has to be bijective. Thus a logic function is logical reversible if there is a one-to-one correspondence between its input and output vectors [20].

Don't Cares are classified into three categories: inputs, outputs, and conditions. When defining logical functions, there are inputs whose corresponding outputs are not determined. That is, the truth table of the function is not completely defined. Conventionally, these patterns are called "don't care conditions". In reversible or quantum logic circuits, there are also some inputs or outputs whose values are not important. These extra inputs or outputs are usually added to the circuit to maintain the reversibility condition. Traditionally, these added inputs and outputs are called "constant inputs" and "garbage outputs", respectively. Constant inputs are some inputs of a reversible or quantum circuit with arbitrary constant values [21].

It is proved that there is an optimum value for number of constant inputs to obtain a circuit with minimum quantum cost [22]. To make the logical function of the multiplexer design reversible, one constant input R=1 and three garbage outputs (Gar_s) are added to the truth table of MUX 2×1. The reversible truth table of our proposed circuit is shown in table 5.

Table 5. The Reversible Function of the proposed MUX 2×1

R	SEL	A	B	F	Gar1	Gar2	Gar3
1	0	0	0	X	X	X	X
1	0	0	1	X			X
1	0	1	0	X			X
1	0	1	1	X		…	X
1	1	0	0	X		…	X
1	1	0	1	X			X
1	1	1	0	X			X
1	1	1	1	X	X	X	X
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	1	0	0	1
1	0	1	1	1	0	1	1
1	1	0	0	0	1	0	0
1	1	0	1	1	1	1	0
1	1	1	0	0	1	0	1
1	1	1	1	1	1	1	1

The output functions of the proposed Reversible MUX are defined as follow:

$$\begin{cases} F = A\overline{SEL} + BSEL \\ Gar1 = SEL \\ Gar2 = B \\ Gar3 = AR \end{cases}$$

QCA implementation of the proposed Reversible MUX design is shown in Figure 8. The proposed design totally applies 4 Majority gates. Two AND gates for ANDing two inputs with the selection line and One OR gate to add them. One additional AND gate is used to produce garbage output Gar3. Two clocking zones are only used and the number of QCA cells is minimal in the layout of the design. The proposed design resulted in decrease in cell counts and decrease in input to output delay and increase in speed. Implementation of three proposed reversible MUXs 2×1 with occupied rectangular area 11×11 cells results in the entire layout of 11×39 cells in the test layer.

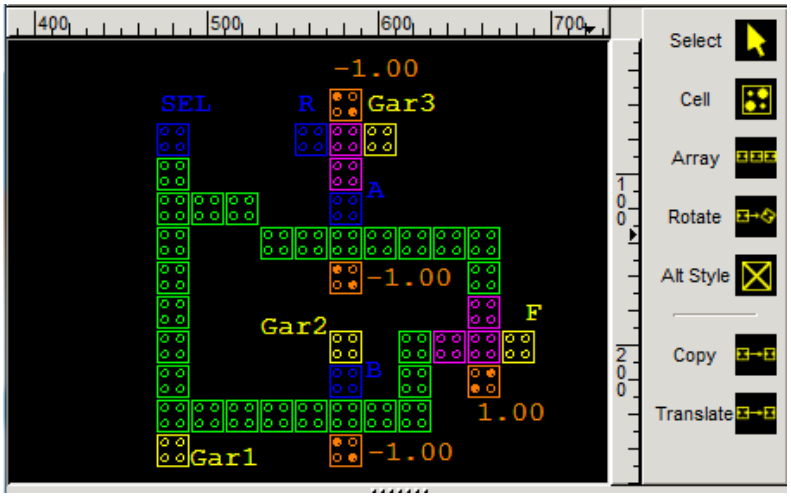

Figure 8. QCA Implementation of the Proposed Reversible MUX 2×1 Design

3.4 Simulation for Functional Verification

All the designs were verified using QCA Designer version 2.0.3 [24]. In the Bistable Approximation, the following parameters are used: Cell Size = 18 nm, Number Of Samples = 12800, Convergence Tolerance = 0.001000, Radius Of Effect = 65 nm, Relative Permittivity=12.9, Clock High=9.8e−22, Clock Low= 3.8e − 23, Clock Amplitude Factor = 2.000, Layer Separation = 11.5000 nm, and Maximum Iterations Per Sample = 100. In our proposed QCA layout, implementing a workable design with a compact layout is considered. The simulation result of Fredkin gate is shown in Figure 9. Input U acts as a control signal. The simulation result of our proposed Reversible QCA multiplexer design is shown in Figure 10.

Figure 9. The Simulation Result of Fredkin Gate

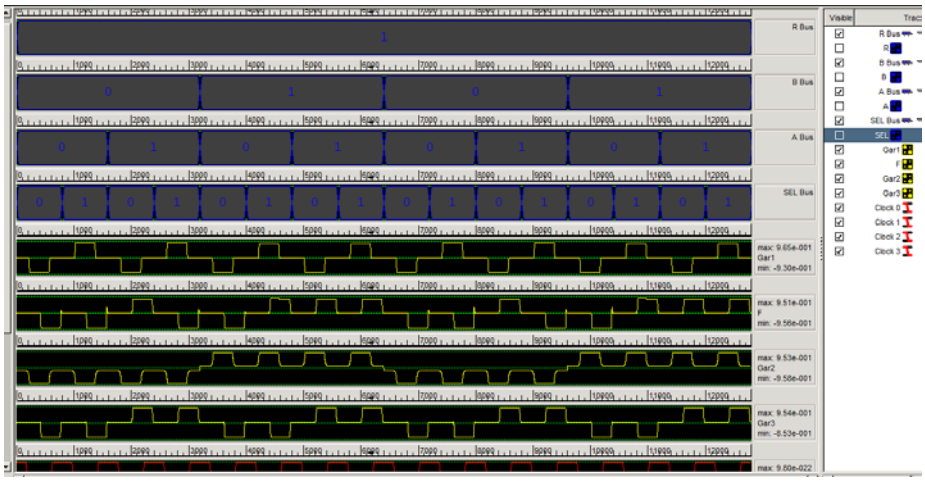

Figure 10. The Simulation Result of the Proposed MUX 2×1 Design

Three Reversible QCA MUXs are compared and the results are shown in Table 6. The number of MV gates and the number of clocking zones are reported. The number of *clocking zones* is presented to quantify the delay between inputs and outputs. The *geometric area*, which in one QCA cell is considered as unit area, occupied by each gate is provided. This is defined as the *rectangular area* occupied by the design. The

number of QCA cells used in each design is also compared. The *control cells* are the input cells with fixed polarization, which are used to program the MV as a 2-input OR, or AND gate. All other cells are referred to as *normal cells*. The clocking scheme is referred to Landauer or Bennett clock.

The majority voter circuit in QCA is reversible under Bennett clocking. But there is a tradeoff between circuit reversibility and therefore energy consumption and circuit delay when selecting a clocking scheme for QCA. Furthermore, the control of Bennett clocking is more complex compared with Landauer clocking [12]. Although MUX has smaller layout, these properties make the implemented test layer slower than using Fredkin gate.

The provided results by comparing designs indicate that our proposed MUX design has demonstrated significant improvements and is more preferable for testable Reversible QCA implementation when considering both circuit area and circuit speed. Proposed implementation of the Reversible MUX 2×1 design uses the minimum number of clocking zones and gates and maximizes the circuit density and focuses on a layout of the circuit which is minimal in using QCA cells. Hence, the proposed design greatly reduces occupied area and delay in signal propagation from input to output. The design is also very simple to implement by QCA cells.

Table 6. Comparison between the Three MUX 2×1 Designs

Parameters	Earlier MUX 2×1	Fredkin gate	Proposed MUX 2×1
Clk Zones	4	4	2
MVs	3	6	4
rectangular Area	14×17	18×30	11×11
Ctrl Cells	3 cells	6 cells	4 cells
Normal Cells	*63 cells*	185 cells	44 cells
Clocking	*Bennett*	Landauer	Landauer

4. Conclusion

In this paper, a testable implementation of Reversible QCA circuits is investigated. A test method regarding to Built In Self Test technique is developed for detecting defects. The partitioning capability and the multilayer property of the QCA circuits are used to establish the test method. All types of defects and a process of providing an exhaustive test set with 100% coverage investigated. A new design Reversible QCA MUX 2×1 is proposed for the test layer implementation regarding to overhead and power savings. The proposed Reversible MUX design has demonstrated significant improvements and uses the minimum number of QCA cells, clocking zones and gates. Hence, the proposed design resulted better area efficiency and less input to output delay and is more efficient and less complex than its classical counterpart.

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