Journal of Advances in Computer Research
Quarterly pISSN: 2345-606x eISSN: 2345-6078
Sari Branch, Islamic Azad University, Sari, I.R.Iran
(Vol. 7, No. 2, May 2016), Pages: 115-125
www.jacr.iausari.ac.ir

A Low-Power and Low-Energy 1-Bit Full Adder Cell Using 32nm CNFET Technology Node

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Received: 2015/07/02; Accepted: 2015/08/18

Abstract

Full adder cell is often placed in the critical path of other circuits. Therefore it plays an important role in determining the entire performance of digital system. Moreover, portable electronic systems rely on battery and low-power design is another concern. In conclusion it is a vital task to design high-performance and low-power full adder cells. Since delay opposes against power consumption, we focus on Power-Delay Product (PDP) as a figure of merit. In this paper using carbon nanotube field-effect transistors (CNFETs) a novel low power and low PDP 1-bit full adder cell is proposed. The novel cell is based on capacitive threshold logic (CTL) and to strengthen its internal signals transmission gates (TGs) are applied. Using both CTL and TG techniques lead to achieving low power consumption full adder cell. Intensive simulations with 32nm technology node using Synopsys HSPICE with regard to different power supplies, temperatures, output loads, and operating frequencies are performed. All simulations confirm the superiority of the proposed cell compared to other state-of-the-art cells.

Keywords: *Nanoelectronics, Carbon Nanotube Field-Effect Transistor (CNFET), Full Adder, Low Power, Low Energy.*

1. Introduction

Full adder cell is one of the most important circuits since it is used as building block of larger circuits such as subtractor, multiplier, divider, and compressor. It is often placed along the critical path of circuits and affects the whole performance of digital systems. Therefore it is important task to design low-power and high-performance 1-bit full adder cells.

Historically transistor dimensions have been scaling down continuously. The number of transistors on an integrated circuit nearly doubles each eighteen month. This is known as Moore's law that has been continued until now [1]. Nowadays technology has reached to the nanoscale dimension. But in nano regime some critical issues for metal-oxide-semiconductor field-effect transistors (MOSFETs) are arisen that limit further shrinking of transistors. For instance, decreased gate control, increased current leakage, short channel effects, etc., are some of issues for nanoscale MOSFETs [2]. Therefore to overcome the limits of nanoscale MOSFETs, new technologies such as Quantum-Dot Cellular Automata (QCA) [3, 4], Single-Electron Transistor (SET) and Carbon Nanotube Field Effect Transistor (CNFET) were emerged recently. Among these

technologies CNFET is more promising successor to conventional silicon MOSFETs because of its remarkable properties. CNFETs have superior characteristics such as 1-D band structure, ballistic transport operation, and low OFF-current [5-8]. Moreover with the same transistor sizes for p-type CNFET (PCNFET) and n-type CNFET (NCNFET) they have equal mobility that this property makes transistor sizing of complex circuits easier [9]. Carbon nanotubes (CNTs) used as channel of CNFETs are classified into two groups called single-wall carbon nanotube (SWCNT) and multi-wall carbon nanotube (MWCNT). SWCNTs are promising alternative to traditional MOSFETs because of easier manufacturing process [10].

The integer pair (n_1, n_2) called chirality indicates the arrangement angle of carbon atoms along CNTs. If n_1-n_2=3K (K$\epsilon\mathbb{Z}$) then CNT is metallic and otherwise it is semiconducting. The diameter of CNT is computed using the following Equation [10].

$$D_{CNT} \approx 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (1)$$

The threshold voltage of a CNFET can be adjusted by setting a proper diameter for its CNTs. It is proportional to the inverse of diameter and is computed using Equation (2) [10].

$$V_{th} = \frac{0.43}{D_{CNT}(nm)} \quad (2)$$

In this paper a new full adder cell is presented based on synergic capacitive threshold logic (CTL) and transmission gate (TG) techniques. The CTL technique leads to the reduction of transistors to produce output signals. On the other hand, TG leads to have full swing signals in the internal nodes. In fact we advantage the merits of each technique. These techniques will result in the lower power and energy consumption which is the main target of this work. It is worth to note that the previous designs often use one logic style to realize 1-bit full adder cell.

The reminder of this paper is organized as follows. In section 2 we will review some state-of-the-art 1-bit full adder cells. Then in section 3 the novel design is proposed. In section 4 simulation results are discussed. Finally section 5 concludes the paper.

2. Previous Work

In this section some state-of-the-art full adder cells are reviewed. Since our proposed cell is based on CTL we have selected full adder cells that they are based on CTL.

The structure of Design2 cell is shown in Figure 1 [11]. It consists of seven capacitors and eight transistors. Two conventional inverters are utilized to produce carry out (Cout) signal. The first inverter is a Majority-NOT and the second one realizes Majority function. This technique reduces the number of transistors remarkably. To produce Sum signal the summation of input signals and two times of Majority-NOT signal is used. The inverter gates at the output lead to have signals with driving capability. One handicap of Design2 is that it uses capacitors at internal nodes. Therefore it will be sensitive to voltage scaling.

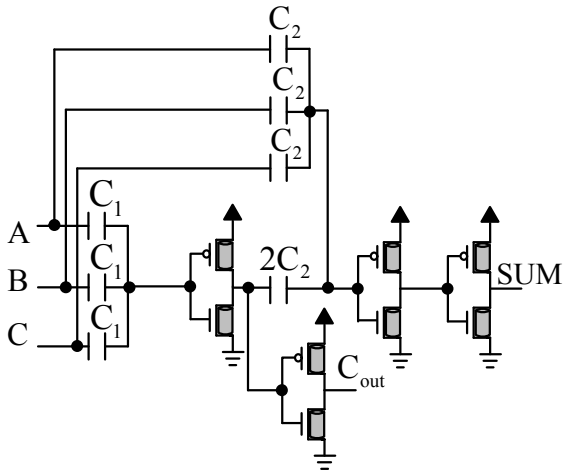

Figure 1. The schematic of Design2 [11]

The structure of 3c2c cell is shown in Figure 2 [12]. In fact it is the enhanced version of Design2 full adder cell. It only applies five capacitors and eight transistors in its structure. The basic idea to produce Sum and Cout signals is similar to that of the Design2 circuit. The same as Design2 it uses capacitors at internal nodes. Therefore it also will be sensitive to voltage scaling. Totally both Design2 and 3c2c designs are sensitive to voltage scaling and will fail to function in cascaded manner.

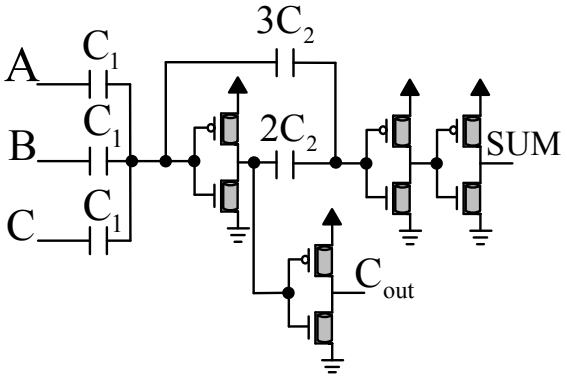

Figure 2. The schematic of 3c2c [12]

Figure 3 shows the structure of full adder cell (FA1) proposed in [13]. The FA1 cell contains fourteen transistors which four of them are placed along maximum critical path of full adder. Therefore the FA1 has a long propagation delay. The FA1 has not driving power and it is expected to show worse performance in the presence of large fanouts.

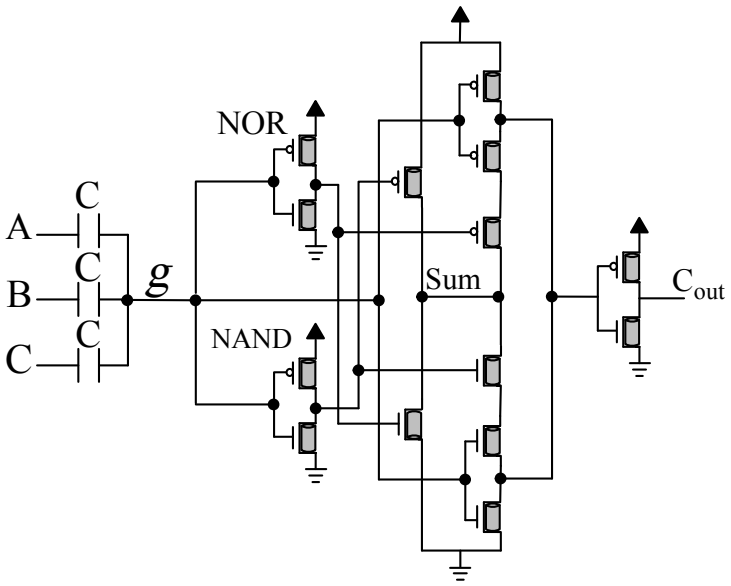

Figure 3. The schematic of FA1 [13]

Figure 4 shows the structure of full adder cell (FA2) proposed in [14]. It consists of twelve transistors and three capacitors. The FA2 cell uses the voltage of capacitor network to control transistors. Therefore, this technique results in increasing of speed of full adder cell. The inverter gates at the output nodes lead to have driving capability. In conclusion, this design will function properly in the presence of large fanouts and cascaded structures.

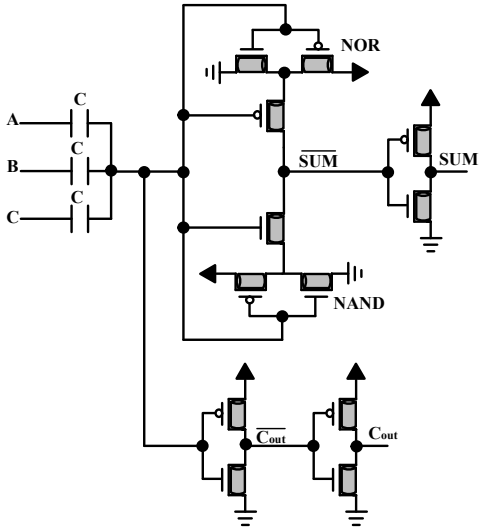

Figure 4. The schematic of FA2 [14]

The structure of the SyMuT full adder cell [15] is shown in Figure 5. The SyMuT consists of fourteen transistors and three capacitors. It uses four independent paths to generate Sum signal. First Cout signal is produced and then using it the Sum signal is produced through four paths. The critical path of SyMuT contains four transistors. The Cout signal is produces using two cascaded inverters but the Sum signal is produces using four paths. However path transistors are utilized in the four paths, the Sum output is full swing. Therefore SyMuT can drive large fanouts.

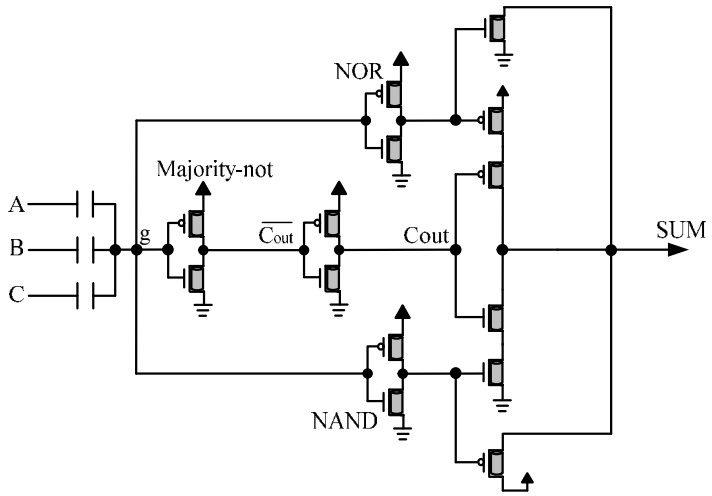

Figure 5. The schematic of SyMuT [15]

3. Proposed Full Adder

The proposed full adder cell is based on the following equations. First complement of Sum and Cout signals are produced. Then using two inverter gates non complement signals are produced. Presence of inverters improves driving capability of the proposed cell.

$$\begin{aligned} \overline{Cout} &= \overline{A}(\overline{B.C}) + A(\overline{B+C}) \\ \overline{Sum} &= \overline{(\overline{B+C})}.(\overline{B.C}).A + \overline{(\overline{B.C})}.\overline{A} + \overline{(B+C)}\,\overline{A} \end{aligned} \tag{3}$$

The transistor level implementation of the proposed cell is shown in Figure (6). In order to make internal signals more strength, TGs are used. To realize TGs for Sum signal we use the potential of capacitor network. TGs improve performance of the proposed circuit. The proposed cell consists of 22 transistors and two capacitors. The maxim critical path of the proposed cell consists of three transistors.

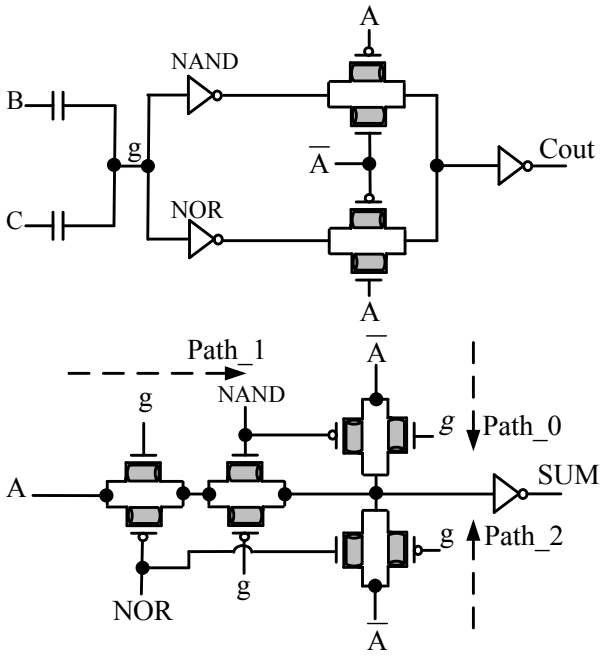

Figure 6. The schematic of the proposed full adder

To produce Cout output, first 2-input NAND and NOR functions are generated using CTL and input signals of B and C. Then, these functions are multiplexed by input signal A. To produce Sum signal three different paths are applied called path_0, _1, and _2. Table 1 tabulates how these paths produce complement of Sum signal. For instance, if input signals are BC=01 then outputs of NAND and NOR functions are logic 1 and logic 0 respectively. Then path_0 and path_2 become high-impedance. In this situation only path_1 is active and applies input A to $\overline{Sum}$ signal. Finally the inverter gate existence in the last stage produces Sum signal from its complement.

Table 1. States of different paths of $\overline{Sum}$ signal

B	C	NAND	NOR	Active Path	$\overline{Sum}$
0	0	1	1	0	$\overline{A}$
0	1	1	0	1	A
1	0	1	0	1	A
1	1	0	0	2	$\overline{A}$

4. Simulation Results

In this section we first propose the simulation environment. Then we perform intensive computer simulations to study the figure of merit of the proposed cell compared to other ones. Simulations against various power supplies, temperatures, output loads, and operating frequencies are performed.

4.1. Simulation Environment

We have used Synopsys HSPICE tool in order to perform simulations. The 32nm Compact SPICE model presented in [16, 17] is used. This model is developed for MOSFET-like CNFETs with SWCNTs as their channel and considers nonidealities

such as Parasitics including CNT, Source/Drain, Gate resistances and capacitances, and Schottky Barrier Effects.

Figure 7 illustrates the simulation test bed [18] with standard fanout of four inverters (FO4) at the output nodes. All 56 possible input transitions are fed to the circuit through buffers. Buffers help to have more realistic input patterns. The delay of output signals is measured from the time that input signals before the buffers reach to 50% of their voltage level to the moment that output signals reach to the same level. Then the maximum delay is reported as the delay of the circuit. The power consumption is the average power consumption measured during a long time. Finally power-delay product (PDP) since compromises between delay and power consumption is reported as a figure of merit. Transistors are sized such that the minimum PDP is reached. In order to obtain the minimum PDP we have used algorithm proposed in [19].

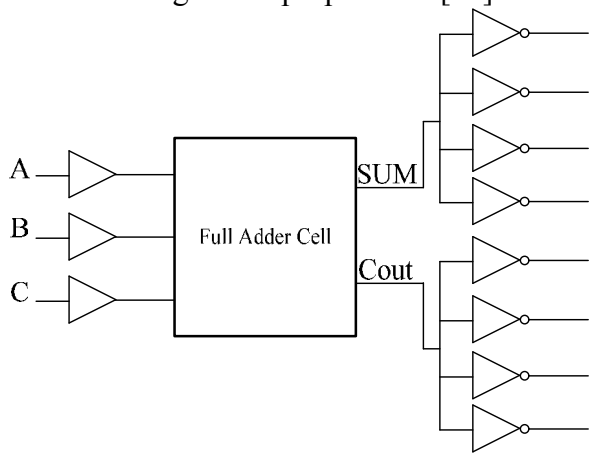

Figure 7. Simulation test bed

4.2. Power Supply Variation

The effect of power supply scaling on the performance metrics of full adders is studied in this subsection. Simulation is done at 100MHz operating frequency, load of FO4, and room temperature (27°C). Simulation results are tabulated in Table 2. Bold-faced numbers show the best results. Considering Table 2 it is apparent that the minimum power consumption and PDP belongs to the proposed full adder cell. The power consumption of the proposed cell is at least 2X better than the other cells. For instance, the proposed cell offers 53% and 55% savings with regard to power and energy consumption, respectively, over SyMuT cell. Among different cells, the FA1 cell has more power consumption because of having non full swing signals at internal nodes. Non full swing signals result in to have static power consumption. Results of this simulation show that the proposed full adder cell scales well with reducing power supply. Moreover, the minimum delay belongs to SyMuT full adder.

Table 2. Delay, Power, and PDP versus power supply variation

Vdd (V)		0.75	0.8	0.85	0.9
Delay (pS)	Design2	78.789	66.913	66.162	68.699
	3c2c	115.84	113.73	116.98	122.27
	FA1	1027.4	218.68	89.471	80.539
	FA2	126.76	76.328	54.150	49.523
	SyMuT	**39.874**	**34.555**	**33.120**	44.796
	Proposed FA	54.304	49.519	45.971	**42.965**
Power (µW)	Design2	0.50033	0.61176	0.8232	1.2269
	3c2c	0.68176	0.84236	1.1162	1.5563
	FA1	0.79202	0.88000	1.0282	1.1455
	FA2	0.34011	0.43584	0.57609	0.81418
	SyMuT	0.24837	0.34109	0.45429	0.66322
	Proposed FA	**0.17363**	**0.20332**	**0.25228**	**0.30623**
PDP (fJ)	Design2	0.03942	0.04093	0.05446	0.08428
	3c2c	0.07897	0.09579	0.13057	0.19028
	FA1	0.81368	0.19244	0.09199	0.09225
	FA2	0.04311	0.03326	0.03119	0.04032
	SyMuT	0.009903	0.01178	0.01504	0.02970
	Proposed FA	**0.009428**	**0.01006**	**0.01159**	**0.01315**

4.3. Temperature Variation

Temperature noise is one of the most important issues which negatively affect the performance of the circuit. We have studied robustness of cells against temperature noise at 100MHz frequency, load of FO4, 0.9V power supply and temperatures in the range of 0°C to 70°C. Simulation results are shown in Figure 8. Figure 8 clarifies that the proposed cell functions well against temperature variations and has the minimum PDP compared to other full adders. Among different cells 3c2c, FA1 and Design2 have the highest PDP, respectively. Therefore they are not good to be used in low power applications.

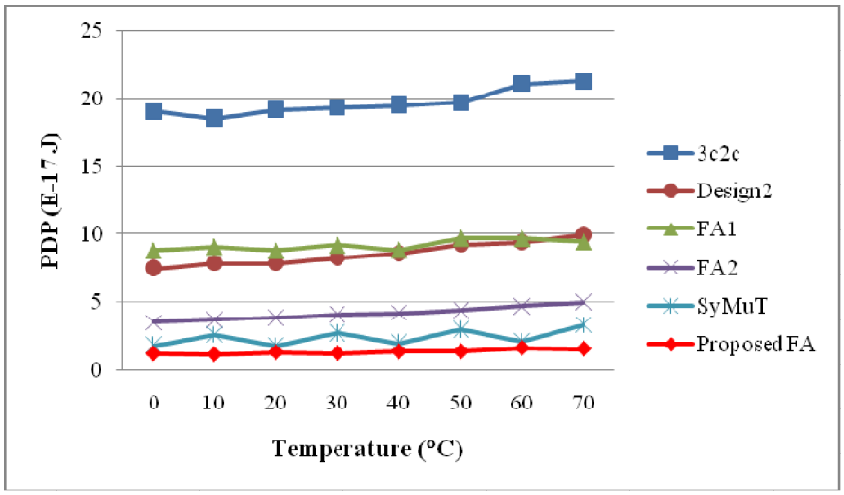

Figure 8. PDP versus temperature

4.4. Load Variation

Since full adder cells are placed in larger circuits with larger output loads, we have studied performance of cells against different loads ranged from 2fF to 10fF. Simulation results are shown in Figure 9. It is worth to note that the FA1 and 3c2c have the highest PDP. The FA1 has not driving power for Sum output. Therefore, it will not function well in the presence of large fanouts. The 3c2c cell has high PDP because of applying capacitor at internal nodes. The non full swing logic levels result in producing of static power consumption and consequently more energy consumption. Therefore they are not suitable to be used in larger circuits. Results depict that the minimum PDP belongs to the proposed cell at all output loads. This is because of applying both TG and inverter gates at output nodes. For instance, the proposed cell offers about 14% better PDP compared to SyMuT which is the best adder after the proposed one at 10fF load.

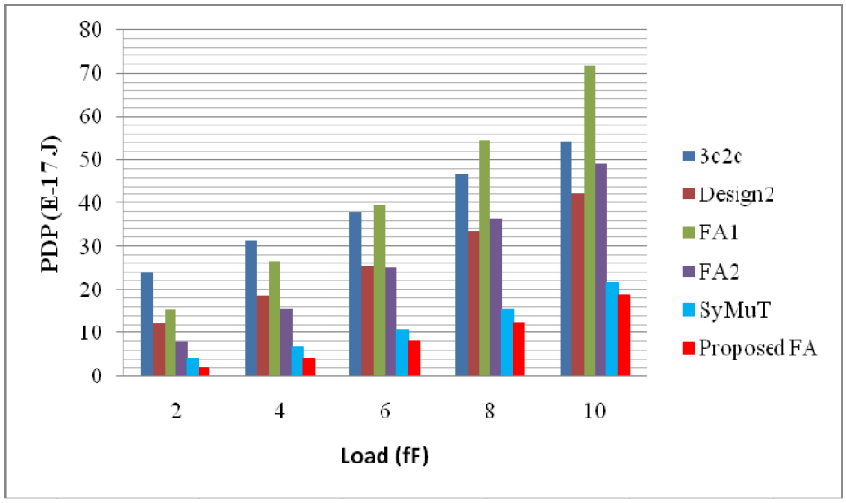

Figure 9. PDP versus output load

4.5. Frequency Variation

Today high frequency operation is a demand for electronic devices. To study the speed of cells we have performed simulation in the presence of different operating frequencies ranged from 1GHz to 2.5GHz, at 0.9V power supply, load of FO4, and room temperature. Figure 10 shows simulation results. Results demonstrate that the proposed full adder cell can function well with minimum energy consumption. On the other hand the worst PDP belongs to 3c2c and FA1 cells. Therefore the proposed cell is a good choice where high-speed operation is a critical demand.

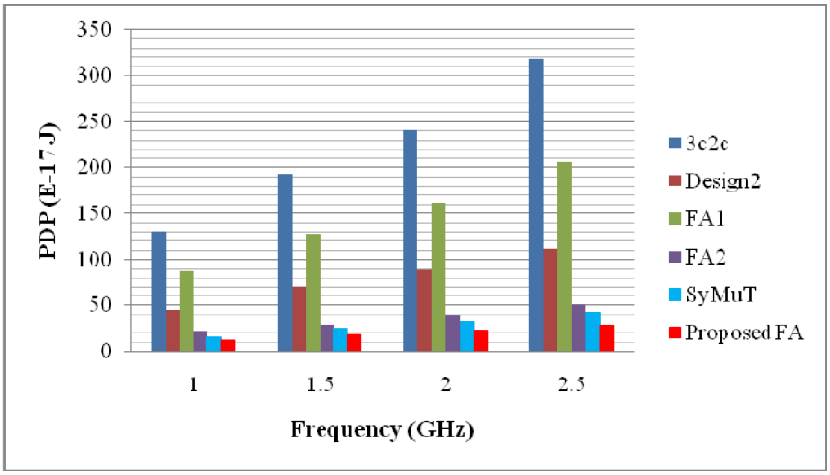

Figure 10. PDP versus frequency

5. Conclusion

Full adder cell is one of the most important circuits because of its effect on the entire performance of the digital system. In this paper a novel 1-bit full adder cell was presented using capacitive threshold logic (CTL) and transmission gates (TGs). Employing these techniques reduced its power consumption remarkably. The proposed cell had twenty two transistors and two capacitors. Its critical path consisted of only three transistors.

The proposed cell was simulated using Synopsys HSPICE tool with 32nm CNFET Compact SPICE model. To study the performance of the proposed cell comprehensive simulations with regard to power supply, output load, temperature noise, and different operating frequencies were done. Simulation results confirmed the superiority of the proposed cell compared to other state-of-the-art full adder cells.

Acknowledgments

This paper is based on the results of a research project named “Design and Transistor Level Implementation of a Full Adder Cell with Low Energy Consumption using Carbon Nanotube Technology” which the authors did with the financial support of Ayatollah Amoli Branch, Islamic Azad University, Amol, Iran.

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