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Design and Implementation of MOSFET Circuits and CNTFET, Ternary Multiplier in the Field of Galois

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Abstract

During the past times, mostly the MOSFET transistor had been used for the design and implementation of the digital integrated circuits for the reason that they were compact, they have the less power consumption and delay to the other transistors. Among the MVL, Ternary Multiplier field because of less evaluated cost of installation and the simple method for implementation of the electronic circuits are considered more than the other ones. In this article, the multiplier circuits based on MOSFET transistor as well, the CNTFET transistor by the use of Ternary Multiplier field of Galois were designed and implemented by Hspice. We have obtained the behavior of this power and delay of these circuits in different temperatures and voltages by controlling the related threshold, and also we have gained the deviation percentage of the average for these two parameters.

Keywords: *Galois; Ternary Multiplier; CNTFET; MOSFET; Field Effect Transistors; Carbon Nano-Tubes.*

1. Introduction

During the past times, the Metal oxide silicon field effect transistors (MOSFET) had been used for the design and implementation of the digital integrated circuits because they are compact and also they have the less consumption power and delay to the other transistors.

But after discovering the carbon nano-tubes by Ijima et al. [1], [2] and [3], several studies have been done on these structures in the other sciences. Therefore, the Carbon nanotube field-effect transistors is a special MOSFET which is very important and the basis of diagram block of Integrated circuits. So, studying the Carbon nanotube field-effect transistors and understanding and comprehending its behavior are two vital subjects to technology and the future of electronics.

Single cover nano-tubes due to the electrical traits such as low consumption power, high speed, the compact area with the smallest dimensions in the form of nano by the unique configuration, multiple threshold recognition, least threshold of noise, etc. better than the other nano-tubes [1], [2] and [3].

MVL circuits have lower power consumption, lower data transfer and also the simpler operations than the binary logic circuits. Due to the features such as high speed in the transfer of information, the decrease of operation, The MVL circuits use less number of gates than the binary logic circuits. Thus using MVL will reduce the connections and more information will be processed than a binary element.

The threshold voltage of MOSFET was calculated based on a channel as the threshold voltage for channel N and channel P is being obtained from the equation (1) and (2), respectively. The threshold voltage of MOSFET has a general equation (3):

$$V_t = \phi_m - x - \frac{E_G}{2q} + \left|\phi_f\right| + \frac{\sqrt{2qk_s\varepsilon.N_B(2\left|\phi_f\right| + V_{SB})}}{C_o} - \frac{\phi_{tot}}{C_o} \quad (1)$$

$$V_t = \phi_m - x - \frac{E_G}{2q} - \left|\phi_f\right| - \frac{\sqrt{2qk_s\varepsilon.N_B(2\left|\phi_f\right| - V_{SB})}}{C_o} - \frac{\phi_{tot}}{C_o} \quad (2)$$

$$V_t = \phi_{ms} + 2\phi_f + \frac{\phi_b}{C_{ox}} + \frac{\phi_{ss}}{C_{ox}} \quad (3)$$

Where $\emptyset_{ms}$ is the differential between work/labor function in the gate of silicon and substrate; $\emptyset_f$is the penetration between the form level and innate energy level in substrate P under the oxide gate; $\emptyset_b$ is the load of empty layer; C_{ox} is the capacity in the oxide level and $\emptyset_{ss}$ is the density of surface. For the simplicity of the work, the equation (4) is used. V_{t0} will be set during the inserting the additional impurities in the area of channel. When V_{t0} as the threshold voltage is $V_{SB} = 0$, γ (gamma) as the parameter of threshold voltage will be defined by the following expression:

$$V_t = V_{t'} + \gamma(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}) \quad (4)$$

$$\gamma = \frac{1}{C_{ox}}\sqrt{2q\varepsilon N_A} \quad (5)$$

If there is $\emptyset_{dep}$ in the area of discharge or it is based on equation (6), so it is possible to use equation (7) as the simplified equation for calculating the threshold voltage of MOSFET.

$$\phi_{dep} = \frac{1}{C_{ox}}\sqrt{4q\varepsilon_{si}\left|\phi_f\right|N_{SUB}} \quad (6)$$

$$V_t = \phi_{ms} + 2\phi_f + \frac{\phi_{dep}}{C_{ox}} \quad (7)$$

Single cover nano-tubes due to the electrical traits such as low consumption power, high speed, the compact area with the smallest dimensions in the form of nano by the unique configuration, multiple threshold recognition, least threshold of noise, etc. better than the other nano-tubes [4], [5], [6], [7], [8], [9] and [10]. An equation (8) is the general equation for calculating the diameter of nano-tube. So, we can write it as a simple one: (9) [11]. "a" is the constant of grafit network which is about 0.249 nm. N1 and N2 are the positive integers which determine the chirality of the nano-tube (inductive and semi-inductive). The threshold voltage of carbon nano-tubes field effect transistors (CNTFET), which is accounted as the half of a band-gap, can be calculated through equation 10. Parameter $v_\pi(\approx 3.033eV)$ must be considered [12], [13] and [14].

$$D_{CNT} = \frac{a * \sqrt[2]{N_1^2 + N_2^2 + N_1N_2}}{\pi} \quad (8)$$

$$D_{CNT} = 0.0783 \times \sqrt[2]{N_1^2 + N_2^2 + N_1N_2} \quad (9)$$

$$V_{TH} = \frac{0.43}{D_{CNT}(nm)}V \quad (10)$$

The performance and behavior of the power and delay of CNTFET in different temperatures are near to each other. So, in order to study the relationships of deviation – percentage, the average was used. The difference between each temperature and different between each delay are being calculated by the average of power (equation 12) and average of delay (equation 11), respectively:

$$A_{Delay1:n} = Delay_{1:n} - Average_{Delay} \quad (11)$$

$$A_{Power1:n} = Temp_{1:n} - Average_{Power} \quad (12)$$

At the end, the obtained difference in each delay and difference will be multiplied in 100 and the final result will be divided into the average of delay (equation 13) or the average of power (equation 14). The gained values are the deviation – percentage from the average of delay and power which are shown in a table. These tables are presented in section 4.

$$\%B_{Delay1:n} = (A_{Delay1:n} * 100) / Average_{Delay} \quad (13)$$

$$\%B_{Power1:n} = (A_{Power1:n} * 100) / Average_{Power} \quad (14)$$

2. Multiplication Circuits

In this paper, by the use of ternary -valued field of Galois, the multiplier circuits based on MOSFET as well, the transistors of field effect of MOSFET-like CNTFET [15], [16], [17], and [18] were designed and implemented. Over the past times, bi-valued logic was used but these days, multi-valued logic (due to the features such as high speed in the transfer of information, decrease of the number of gate, the decrease of operation, etc.) is being used [19], [20].

These circuits were designed and implemented in the field of Galois were shown in table 1. As was shown in figure (1-a), the Ternary Multiplier circuit in the field of Galois which was designed based on the MOSFET transistor was presented in this paper. And also the Ternary Multiplier circuit in the field of Galois which was designed based on the CNTFET transistor was presented in figure (1-b) [20].

The designed circuits with silicon and carbon nano-tubes were implemented for voltage 1 volt and two voltages of 1 and 0.9, respectively. Delay, power and the percentage of deviation from the average of delay and power of these triple circuits were considered in the temperatures of 0, 10, 20, 30, 40, 50, 60, 70, 80, 90 and 100°C.

By controlling the threshold voltage of transistors of field effect in the multiplication and addition circuits, a triple model was designed and implemented. In such designs, resistances of 100K were used.

Table 1: accuracy of multiplication.

Multiplication	0	1	2
0	0	0	0
1	0	1	2
2	0	2	1

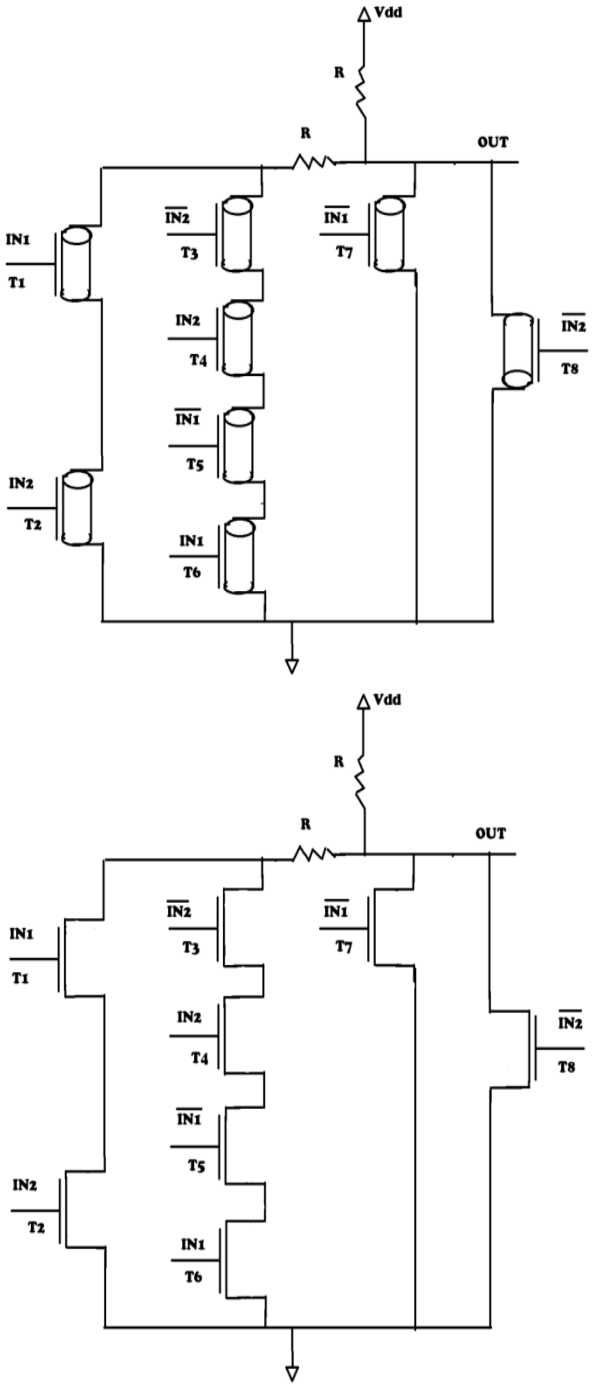


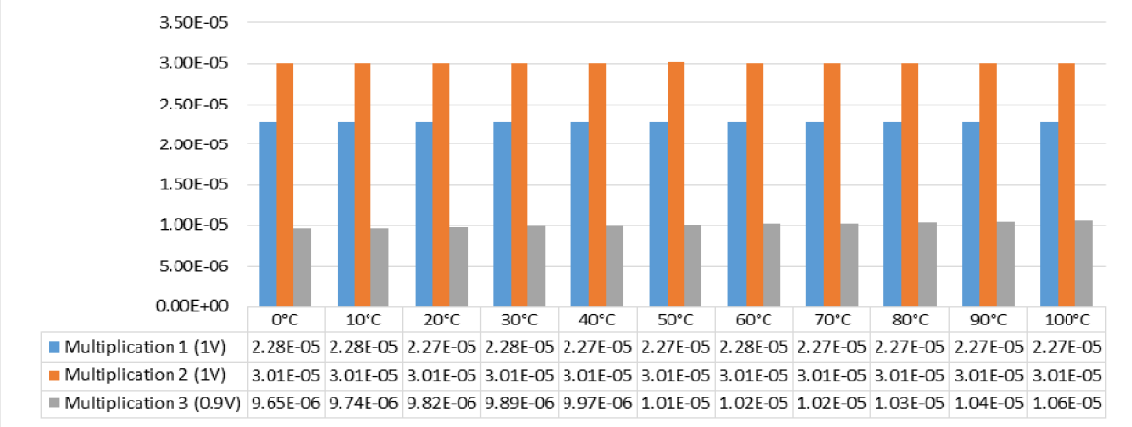
Figure 1: a- implemented multiplication circuits with the MOSFET. b- implemented multiplication circuits with the CNTFET [20].

3. Power of the Multiplication Circuits in the Field of Galois

The power consumed is one of the most important parameters in integrated circuits. So, the power and percentage of deviation from the average of circuit power "MOSFET circuit" was compared with CNTFET.

The related results of power were shown in figure 2. In this fig, Multiplication 1 and Multiplication 2 show the multiplication circuit which was designed by CNTFET (with

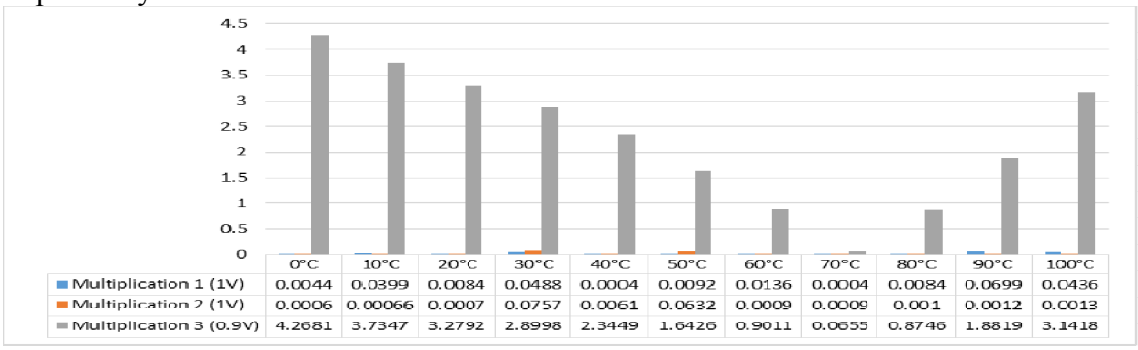
voltage 0.9 and 1) and also Multiplication 3 is about the multiplication circuit of silicon with the voltage of 1 volt. Based on these results, silicon circuits is less and better than the CNT one.



	0°C	10°C	20°C	30°C	40°C	50°C	60°C	70°C	80°C	90°C	100°C
Multiplication 1 (1V)	2.28E-05	2.28E-05	2.27E-05	2.28E-05	2.27E-05	2.27E-05	2.28E-05	2.27E-05	2.27E-05	2.27E-05	2.27E-05
Multiplication 2 (1V)	3.01E-05	3.01E-05	3.01E-05	3.01E-05	3.01E-05	3.01E-05	3.01E-05	3.01E-05	3.01E-05	3.01E-05	3.01E-05
Multiplication 3 (0.9V)	9.65E-06	9.74E-06	9.82E-06	9.89E-06	9.97E-06	1.01E-05	1.02E-05	1.02E-05	1.03E-05	1.04E-05	1.06E-05

Figure 2: power of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperatures of 0, 10, 20, 30, 40, 50, 60, 70, 80, 90 and 100°C.

Based on the presented equations in the introduction section, percentage of deviation from the average of powers for the multiplication circuits were shown as their results were presented in figure 4. Based on these, the deviation-percentage of silicon circuit is high. The average of deviation-percentage from the power of the circuits of Multiplication 1, Multiplication 2 and Multiplication 3 are 0.0225, 0.0139 and 2.276%, respectively.



	0°C	10°C	20°C	30°C	40°C	50°C	60°C	70°C	80°C	90°C	100°C
Multiplication 1 (1V)	0.0044	0.0399	0.0084	0.0488	0.0004	0.0092	0.0136	0.0004	0.0084	0.0699	0.0436
Multiplication 2 (1V)	0.0006	0.00066	0.0007	0.0757	0.0061	0.0632	0.0009	0.0009	0.001	0.0012	0.0013
Multiplication 3 (0.9V)	4.2681	3.7347	3.2792	2.8998	2.3449	1.6426	0.9011	0.0655	0.8746	1.8819	3.1418

Figure 3: Results for the deviation percent of the average power of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperatures 0, 10, 20, 30, 40, 50, 60, 70, 80, 90 and 100°C.

4. Delay of Multiplication Circuits in the Field of Galois

The delay is one of the most important parameters in integrated circuits. So, the power and percentage of deviation from the average of circuit power "MOSFET circuit" was compared with CNTFET.

The first delay in the temperature of 0°C was obtained. The results of delay were shown in figure 4. Based on these, delay in Multiplication 1 and Multiplication 3 is less but in Multiplication 2 is high. As mentioned before, this circuit is in the temperature of 1 volt. So, the least delay was occurred in voltage 1 for the circuit of MOSFET and voltage 0.9 for the circuit of CNTFET.

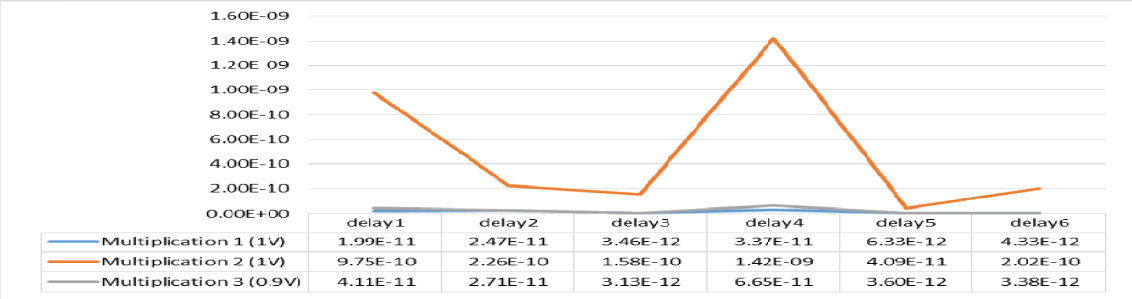


Figure 4: delay of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperature 0°C.

You see the results of deviation-percentage from the average of delay for temperature 0°C in the below table and figure. Percentage of calculated deviation for three circuits means Multiplication 1, 2 and 3 is about 69.418, 91.921 and 86.042%, respectively. So, in this temperature, Multiplication 1 has the least deviation.

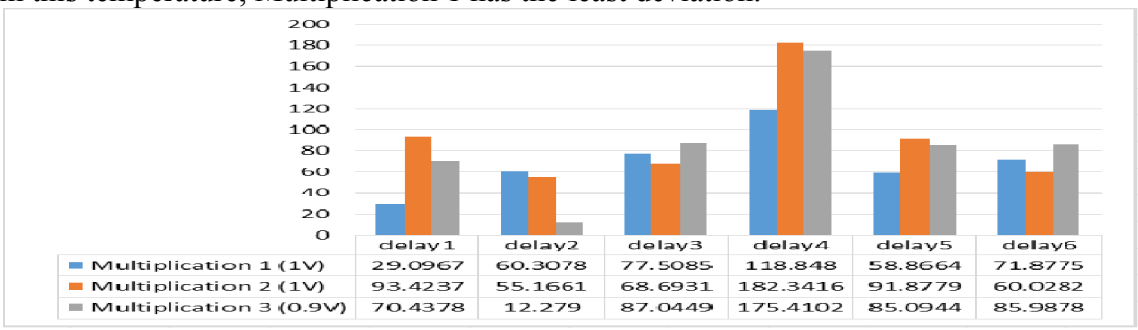


Figure 5: Results for the deviation percent of the average power of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperatures of 0°C.

In this case, figure 6 shows the results of simulation of the multiplication circuits for temperature 10°C. Based on this figure 5 and figure 6, it can be concluded that the silicon circuits has the highest delay. The delay average of this circuit was 1.6E-11. This value for the other two circuits was 1.5E-11 and 1.4E-11, respectively.

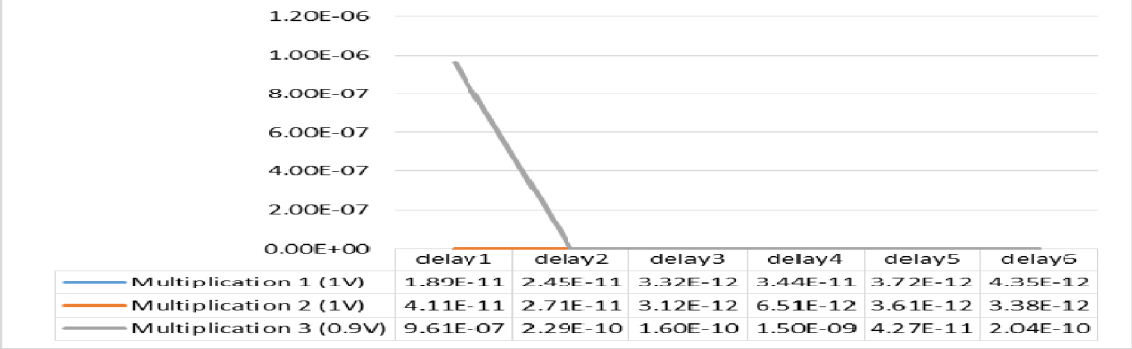


Figure 6: delay of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperature 10°C.

By the use of formula for calculating the deviation-percentage from the averages (of the previous figure), the deviation-percentage of delay average was obtained as its results were presented in figure 7. In such case, circuit Multiplication 3 has the highest temperature. The deviation-percentage from the delay average for these three circuits is about 74.46, 94.16 and 166.22%.

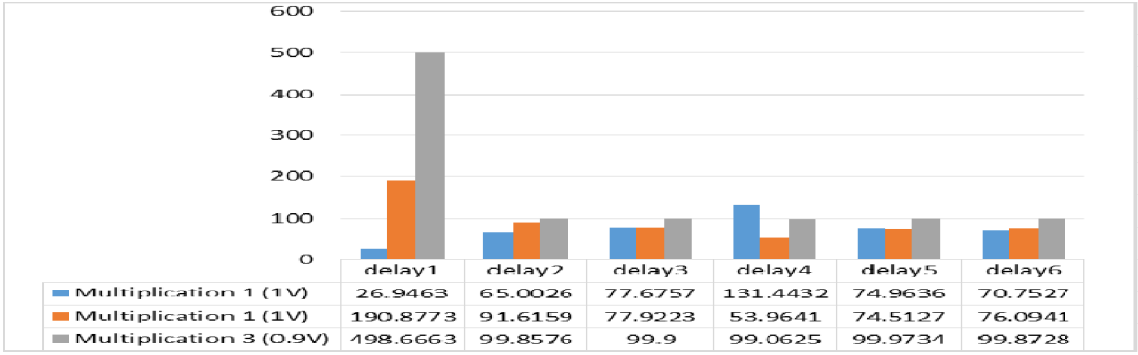


Figure 7: Results for the deviation percent of the average power of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperatures of 10°C.

The delay average for temperature 20°C based on figure 8 shows the least delay of circuits of Multiplication 1 and 2 to the Multiplication 3. Based on the implemented calculations for these three circuits, the delay average was about 1.6E-11, 2.4E-11, and 4.7E-10, respectively.

Figure 8: delay of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperature 20°C.

The deviation-percentage from the delay average of these three circuits (within the temperature of 20°C) is about 67.74, 86.05 and 87.69%. These results are based on figure 9. The least deviation-percentage was allotted to Multiplication 1.

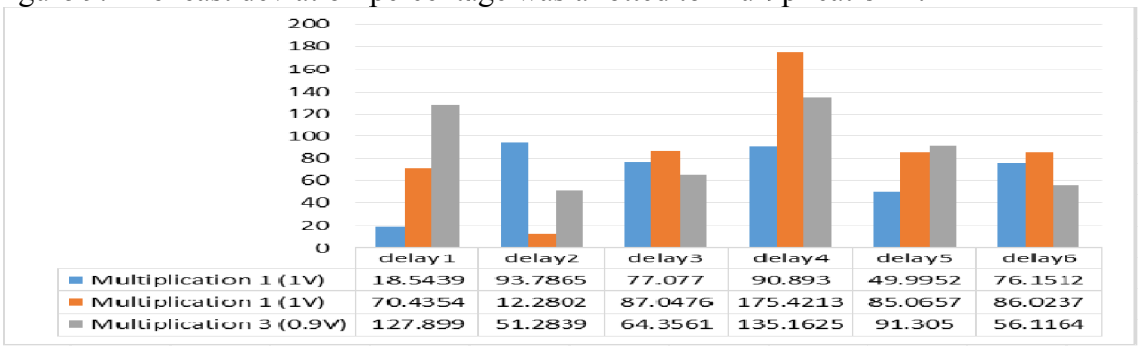
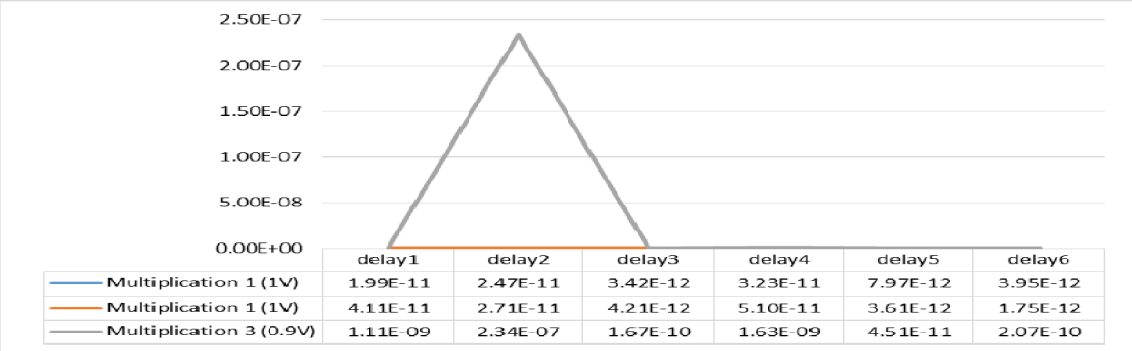


Figure 9: Results for the deviation percent of the average power of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperatures of 20°C.

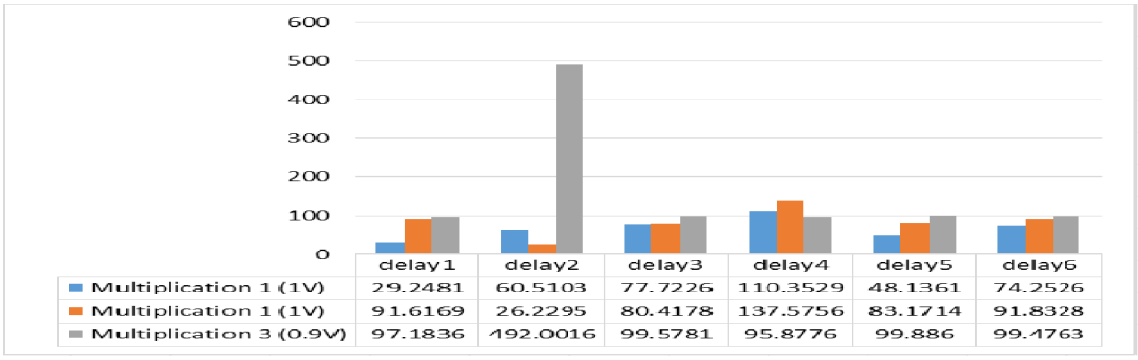
The results of delay within temperature of 30°C were shown in figure 10. The delay average of each circuit was about 1.54E-11, 2.15E-11 and 3.95E-11, respectively. The least deviation-percentage was allotted to CNTFET.



	delay1	delay2	delay3	delay4	delay5	delay6
Multiplication 1 (1V)	1.99E-11	2.47E-11	3.42E-12	3.23E-11	7.97E-12	3.95E-12
Multiplication 1 (1V)	4.11E-11	2.71E-11	4.21E-12	5.10E-11	3.61E-12	1.75E-12
Multiplication 3 (0.9V)	1.11E-09	2.34E-07	1.67E-10	1.63E-09	4.51E-11	2.07E-10

Figure 10: delay of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperature 30°C.

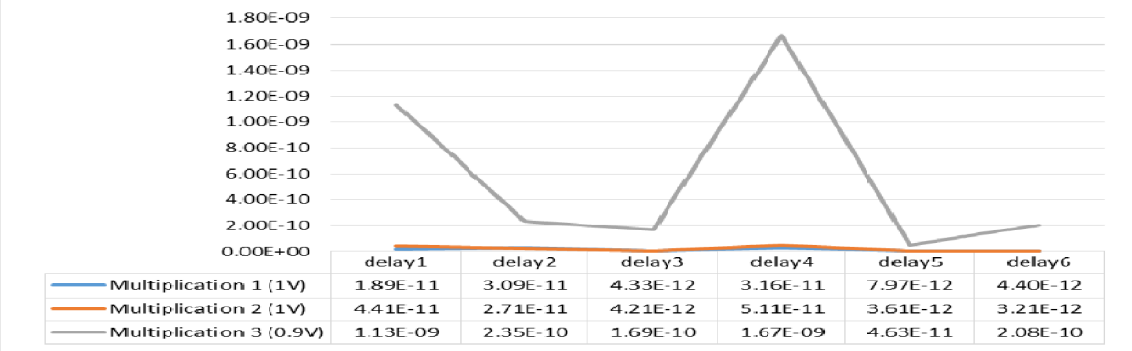
The deviation-percentage from the delay average of these three circuits was calculated based on these equations as its results were shown in figure 11. The deviation-percentage from the delay average of these three circuits (within the temperature of 20°C) is about 66.704, 85.141 and 164.0005%. The most deviation-percentage was allotted to MOSFET.



	delay1	delay2	delay3	delay4	delay5	delay6
Multiplication 1 (1V)	29.2481	60.5103	77.7226	110.3529	48.1361	74.2526
Multiplication 1 (1V)	91.6169	26.2295	80.4178	137.5756	83.1714	91.8328
Multiplication 3 (0.9V)	97.1836	192.0016	99.5781	95.8776	99.886	99.4763

Figure 11: Results for the deviation percent of the average power of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperatures of 30°C.

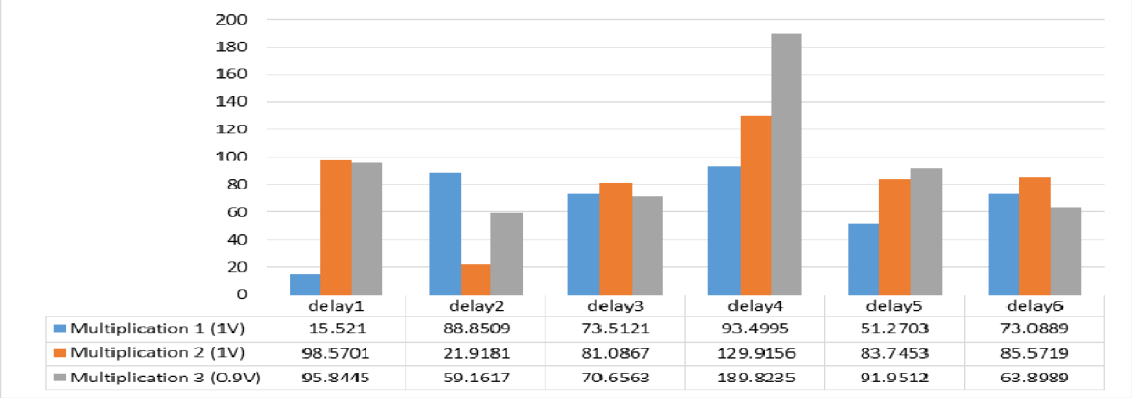
The results of the delays of the implemented circuits within temperature of 40°C were shown in figure 12. The delay average of each circuit was about 1.63E-11, 2.22E-11 and 5.76E-11, respectively. The least deviation-percentage was allotted to CNTFET.



	delay1	delay2	delay3	delay4	delay5	delay6
Multiplication 1 (1V)	1.89E-11	3.09E-11	4.33E-12	3.16E-11	7.97E-12	4.40E-12
Multiplication 2 (1V)	4.41E-11	2.71E-11	4.21E-12	5.11E-11	3.61E-12	3.21E-12
Multiplication 3 (0.9V)	1.13E-09	2.35E-10	1.69E-10	1.67E-09	4.63E-11	2.08E-10

Figure 12: delay of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperature 40°C.

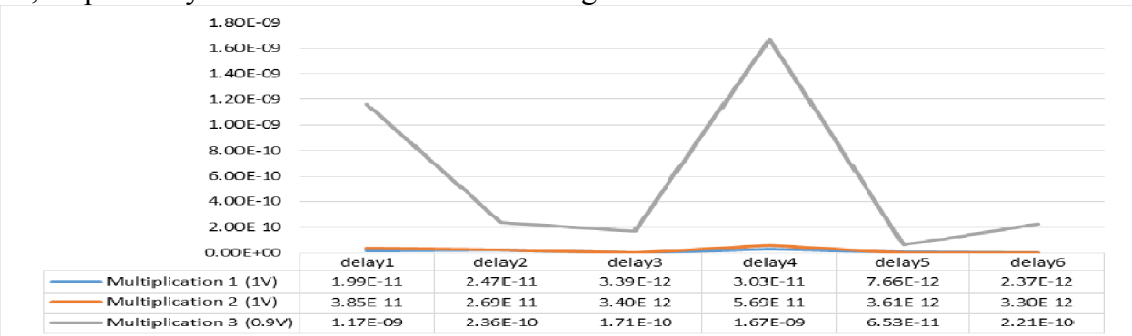
The deviation-percentage is more than the delay average of MOSFET circuit which is about 95.223%. The least deviation-percentage was allotted to Multiplication 1 which was implemented with CNTFET within voltage 0.9. Its percentage average is about 65.957% but for Multiplication 2, it is about 83.468% (Figure 13).



	delay1	delay2	delay3	delay4	delay5	delay6
Multiplication 1 (1V)	15.521	88.8509	73.5121	93.4995	51.2703	73.0889
Multiplication 2 (1V)	98.5701	21.9181	81.0867	129.9156	83.7453	85.5719
Multiplication 3 (0.9V)	95.8445	59.1617	70.6563	189.8225	91.9512	63.8989

Figure 13: Results for the deviation percent of the average power of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperatures of 40°C.

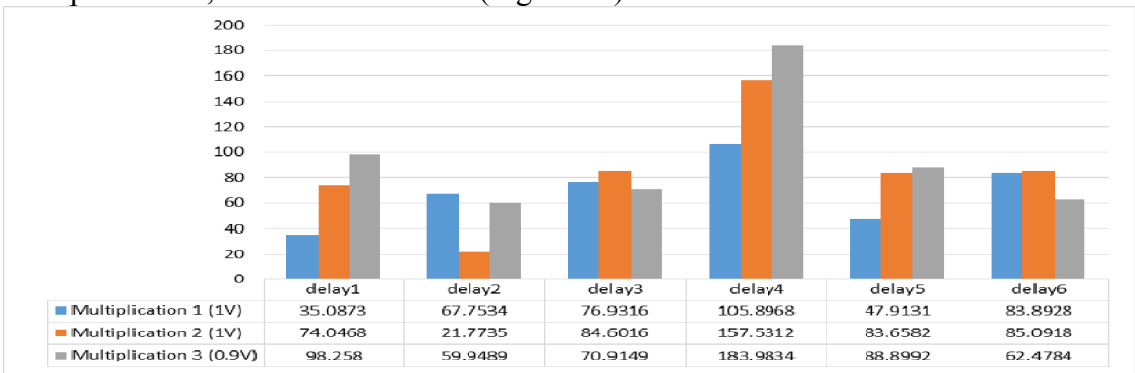
Within temperature of 50°C, the delay of circuits of Multiplication 1 and 2 to the Multiplication 3 is so less. Their delay average is about 1.47E-11, 2.21E-11, and 5.88E-10, respectively. These results are based on figure 14.



	delay1	delay2	delay3	delay4	delay5	delay6
Multiplication 1 (1V)	1.99E-11	2.47E-11	3.39E-12	3.03E-11	7.66E-12	2.37E-12
Multiplication 2 (1V)	3.85E 11	2.69E 11	3.40E 12	5.69E 11	3.61E 12	3.30E 12
Multiplication 3 (0.9V)	1.17E-09	2.36E-10	1.71E-10	1.67E-09	6.53E-11	2.21E-10

Figure 14: delay of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperature 50°C.

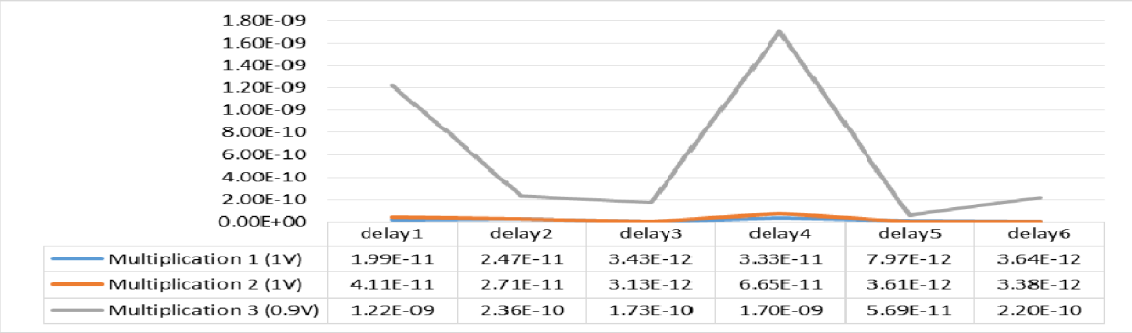
Based on the calculations within temperature of 50°C as temperature of 40°C, the deviation percentage from the delay average of MOSFET circuit is so high which is about 94.080%. The least delay was allotted to Multiplication 1 which was implemented with CNTFET within voltage 0.9. Its percentage average is about 69.579% but for Multiplication 2, it is about 84.451% (Figure 15).



	delay1	delay2	delay3	delay4	delay5	delay6
Multiplication 1 (1V)	35.0873	67.7534	76.9316	105.8968	47.9131	83.8928
Multiplication 2 (1V)	74.0468	21.7735	84.6016	157.5312	83.6582	85.0918
Multiplication 3 (0.9V)	98.258	59.9489	70.9149	183.9834	88.8992	62.4784

Figure 15: Results for the deviation percent of the average power of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperatures of 50°C.

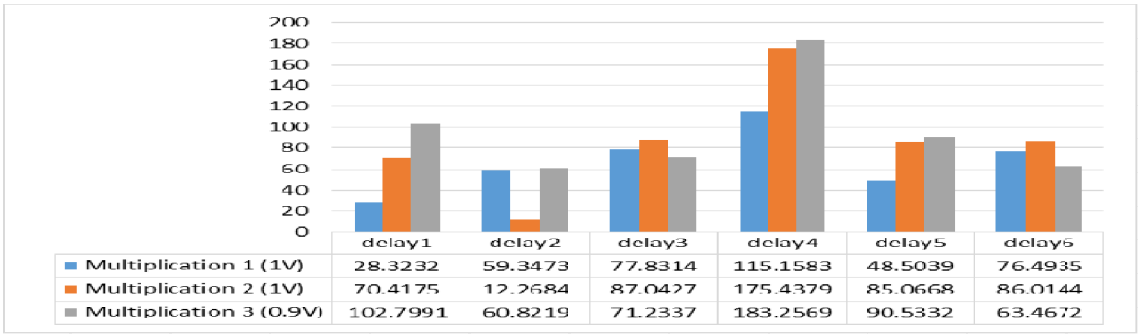
The results of delay within temperature of 60°C as temperature of 50°C for the circuits of Multiplication 1 and Multiplication 2 to Multiplication 3 is so less. Based on figure 16, their delay average about 1.55E-11, 2.41E-11 and 6.10E-10, respectively.



	delay1	delay2	delay3	delay4	delay5	delay6
Multiplication 1 (1V)	1.99E-11	2.47E-11	3.43E-12	3.33E-11	7.97E-12	3.64E-12
Multiplication 2 (1V)	4.11E-11	2.71E-11	3.13E-12	6.65E-11	3.61E-12	3.38E-12
Multiplication 3 (0.9V)	1.22E-09	2.36E-10	1.73E-10	1.70E-09	5.69E-11	2.20E-10

Figure 16: delay of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperature 60°C.

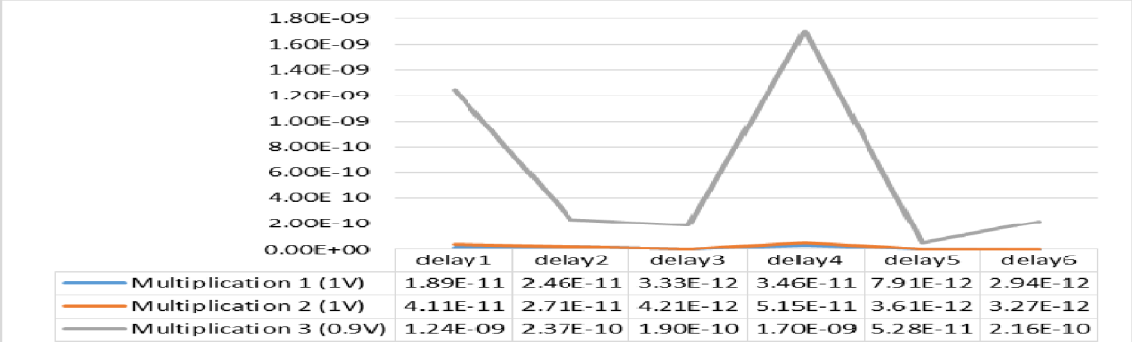
In according to the results of calculations and fulfilled implementation (Figure 17), within temperature of 60°C as previous temperatures, the deviation percentage from the delay average of MOSFET circuit is so high which is about 95.352%. The least delay was allotted to Multiplication 1 (67.609%) as well; the delay of Multiplication 2 is about 86.041%.



	delay1	delay2	delay3	delay4	delay5	delay6
Multiplication 1 (1V)	28.3232	59.3473	77.8314	115.1583	48.5039	76.4935
Multiplication 2 (1V)	70.4175	12.2684	87.0427	175.4379	85.0668	86.0144
Multiplication 3 (0.9V)	102.7991	60.8219	71.2337	183.2569	90.5332	63.4672

Figure 17: Results for the deviation percent of the average power of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperatures of 60°C.

Based on figure 18, delay within temperature of 70°C as previous temperatures, for Multiplication 1 and Multiplication 2 was less (to the Multiplication 3). Based on figure 18, their delay average is about 1.54E-11, 2.181E-11 and 6.07E-10, respectively.



	delay1	delay2	delay3	delay4	delay5	delay6
Multiplication 1 (1V)	1.89E-11	2.46E-11	3.33E-12	3.46E-11	7.91E-12	2.94E-12
Multiplication 2 (1V)	4.11E-11	2.71E-11	4.21E-12	5.15E-11	3.61E-12	3.27E-12
Multiplication 3 (0.9V)	1.24E-09	2.37E-10	1.90E-10	1.70E-09	5.28E-11	2.16E-10

Figure 18: delay of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperature 70°C.

In according to the results of calculations and fulfilled implementation (Figure 19), within temperature of 70°C, the deviation percentage from the delay average of MOSFET circuit is so high (with the average of deviation percentage: 95.121%). Multiplication 1 with the percentage of 69.239% has the least delay; but for multiplication 2, it equals 83.045%.

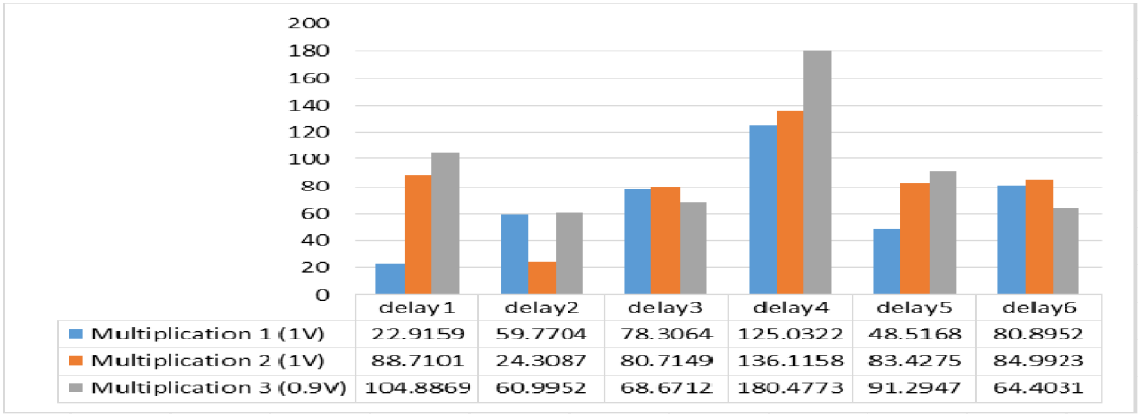


Figure 19: Results for the deviation percent of the average power of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperatures of 70°C.

Based on figure 20, delay within temperature of 80°C for Multiplication 1 and Multiplication 2 was less (to the Multiplication 3). Based on figure 20, their delay average is about 1.52E-11, 2.161E-11 and 6.13E-10, respectively.

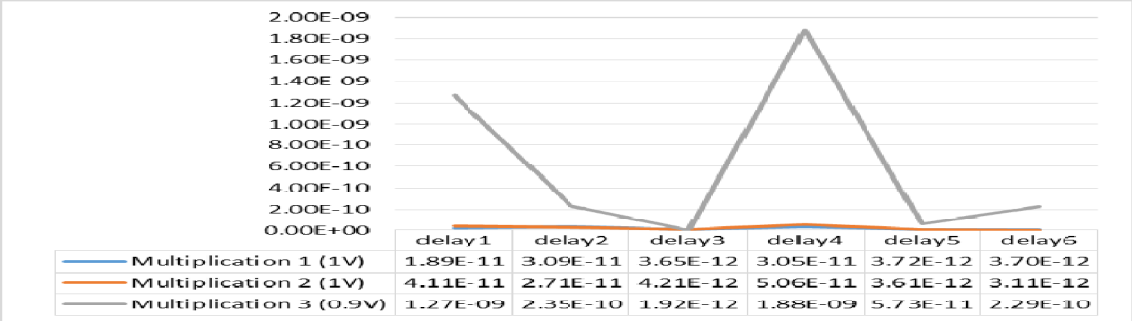


Figure 20: delay of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperature 80°C.

Based on figure 21, the deviation percentage from the delay average of Multiplication 3, in terms of the average of deviation percentage from the average of delay is about 104.854% and it is so high. Circuit Multiplication 1 with the average of 75.737% has the least delay. But for multiplication 2, it equals 83.152%.

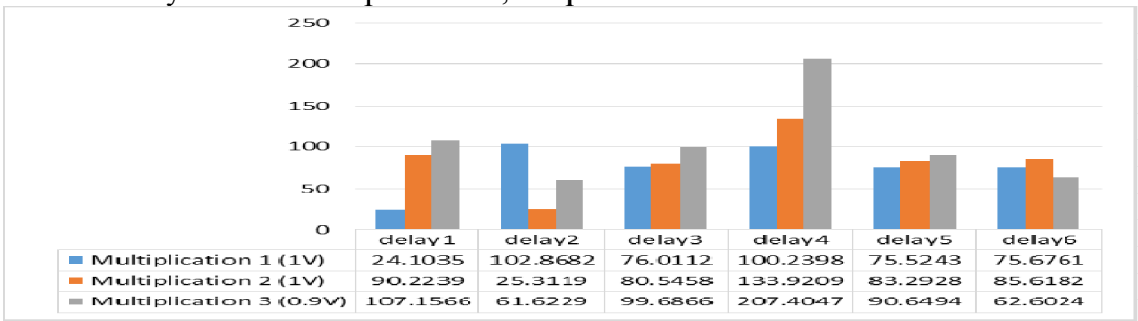
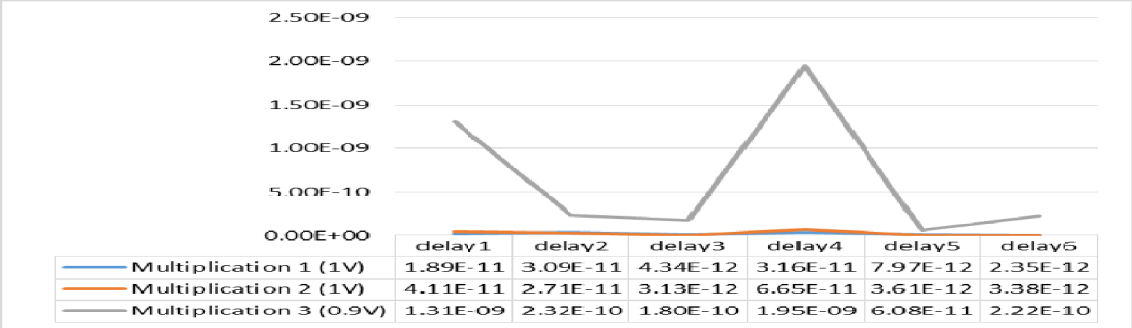


Figure 21: Results for the deviation percent of the average power of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperatures of 80°C.

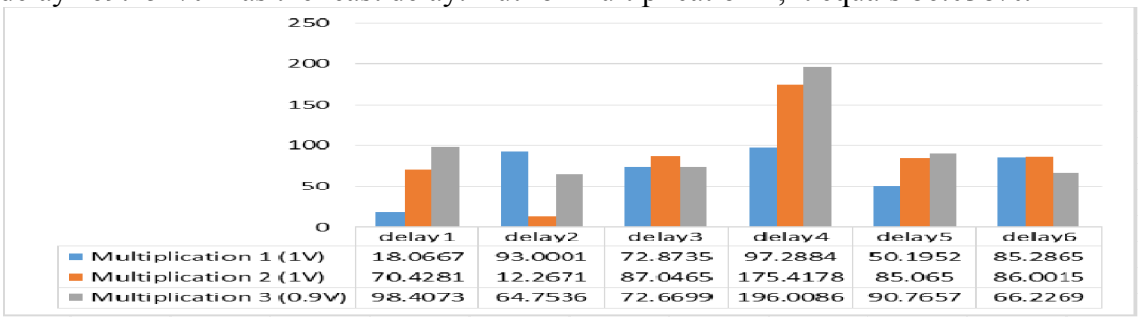
In according to the figure 22 and fulfilled implementation, the delay for Multiplication 1 and Multiplication 1 is less to Multiplication 3. Based on figure 22, the average of their delay was 1.06E-11, 2.41E-11 and 6.58E-10, respectively.



	delay1	delay2	delay3	delay4	delay5	delay6
Multiplication 1 (1V)	1.89E-11	3.09E-11	4.34E-12	3.16E-11	7.97E-12	2.35E-12
Multiplication 2 (1V)	4.11E-11	2.71E-11	3.13E-12	6.65E-11	3.61E-12	3.38E-12
Multiplication 3 (0.9V)	1.31E-09	2.32E-10	1.80E-10	1.95E-09	6.08E-11	2.22E-10

Figure 22: delay of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperature 90°C.

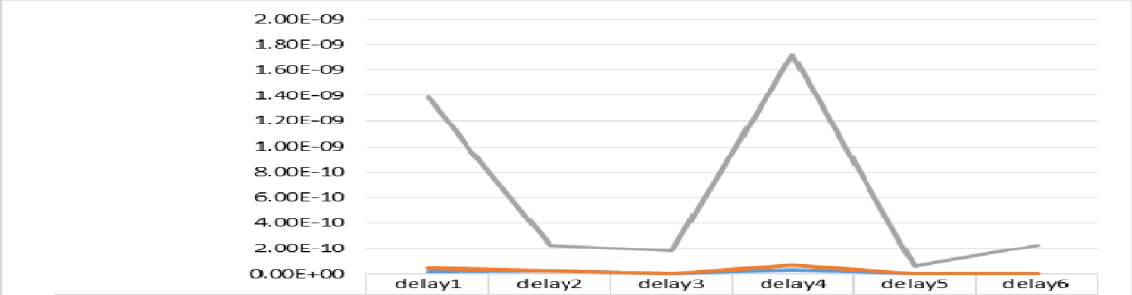
Based on figure 23, deviation percentage from the delay average of Multiplication 3, in terms of the deviation percentage from the average of delay is about 98.139% which is high. Multiplication 1 with the average of deviation percentage from the average of delay "69.452%" has the least delay. But for multiplication 2, it equals 86.038%.



	delay1	delay2	delay3	delay4	delay5	delay6
Multiplication 1 (1V)	18.0667	93.0001	72.8735	97.2884	50.1952	85.2865
Multiplication 2 (1V)	70.4281	12.2671	87.0465	175.4178	85.065	86.0015
Multiplication 3 (0.9V)	98.4073	64.7536	72.6699	196.0086	90.7657	66.2269

Figure 23: Results for the deviation percent of the average power of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperatures of 90°C.

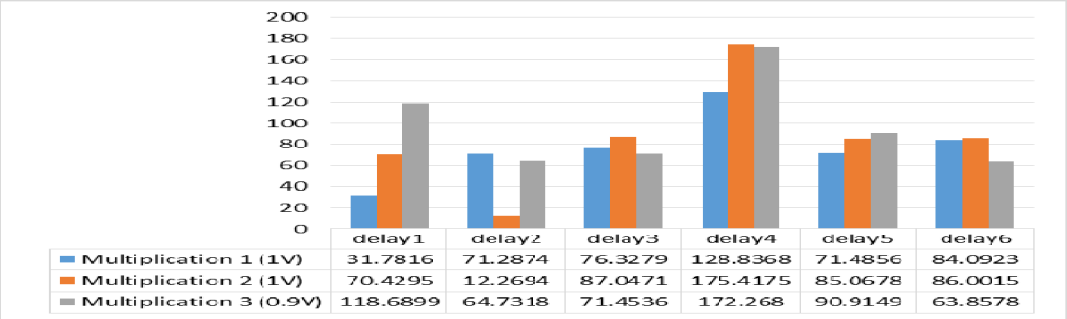
Temperature 100°C is the last case for implementing these three cases as based on the results of the figure 24, delay for Multiplication 1 and Multiplication 2 is less to Multiplication 3. The average of their delay is about 1.43E-11, 2.41E-11and 6.33E-10, respectively.



	delay1	delay2	delay3	delay4	delay5	delay6
Multiplication 1 (1V)	1.89E-11	2.45E-11	3.39E-12	3.28E-11	4.09E-12	2.28E-12
Multiplication 2 (1V)	4.11E-11	2.71E-11	3.13E-12	6.65E-11	3.61E-12	3.38E-12
Multiplication 3 (0.9V)	1.38E-09	2.23E-10	1.81E-10	1.72E-09	5.75E-11	2.29E-10

Figure 24: delay of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperature 100°C.

Based on the last implementation and the results of the figure 25, deviation percentage from the delay average of Multiplication 3, in terms of the deviation percentage from the average of delay is about 96.986% which is high. Multiplication 1 with the average of deviation percentage from the average of delay "77.302%" has the least delay. But for multiplication 2, it equals 86.039%.



	delay1	delay2	delay3	delay4	delay5	delay6
Multiplication 1 (1V)	31.7816	71.2874	76.3279	128.8368	71.4856	84.0923
Multiplication 2 (1V)	70.4295	12.2694	87.0471	175.4175	85.0678	86.0015
Multiplication 3 (0.9V)	118.6899	64.7318	71.4536	172.268	90.9149	63.8578

Figure 25: Results for the deviation percent of the average power of the circuits of Multiplication 1, 2, 3 in voltages of 1 and 0.9 volt for temperatures of 100°C.

5. Conclusion

As evident in the tables and graphs, the least power in the triple field of Galois belongs to the multiplication circuit which was designed and implemented based MOSFET. So, the deviation percentage from the average of the deviation percentage is more than the average of the power of this circuit to them. But the CNTFET in the voltage 0.9 volt showed the least delay and the average of deviation percentage from the average of delay. Therefore, the performance of the power of MOSFET in the three-valued field of Galois is better than the CNTFET.

References

[1] K. Sridharan, S. Gurindagunta and V. Pudi. Efficient Multiternary Digit Adder Design in CNTFET Technology. IEEE Trans, Nanotechnol. 2013.

[2] S.A. Ebrahimi and P. Keshavarzian. Fast low-power full-adders based on bridge style minority function and multiplexer for nanoscale. International Journal of Electronics. 2012.

[3] P. Keshavarzian and M.M. Mohammad. A Novel Efficient CNTFET Gödel Circuit Design. International Journal of Soft Computing and Engineering (IJSCE). PP. 296-300, 2012.

[4] R.D. Levine and F. Remacle. Realization of Complex Logic Operations at the Nanoscale. Architecture and Design of Molecule Logic Gates and Atom Circuits Advances in Atom and single Molecule Machines. pp. 195-220, 2013.

[5] YB. Kim. Challenges for Nanoscale MOSFETs and Emerging Nanoelectronics. Transactions on Electrical and Electronic Materials. Vol. 11, pp. 93-105, 2010.

[6] S. A. Ebrahimi and P. Keshavarzian. Fast low-power full-adders based on bridge style minority function and multiplexer for nanoscale, International Journal of Electronics. Vol. 100, pp. 727-745, 2012.

[7] G. Cho and F. Lombardi. A novel and Improved Design of a ternary CNTFET-based Cell, in GLSVLSI'13. Proceedings of the 23rd ACM International Conference on Great Lakes symposium on VLSI. pp. 131-136, 2013.

[8] P. Junsangsri and F. Lombardi. Design of a hybrid memory cell using memristance and ambipolarity. IEEETrans, Nanotechnol. pp. 71-80, 2013.

[9] K. Sridharan, S. Gurindagunta and V. Pudi. Efficient Multiternary Digit Adder Design in CNTFET Technology. IEEE Trans, Nanotechnol. pp. 283–287, 2013.

[10] S. Lin, Y. Kim and F. Lombardi. Design of a Ternary Memory cell Using CNTFETs. IEEE TRANSACTIONS ON NANOTECHNOLOGY. pp. 1019-1025, 2012.

[11] M. HosseinMoaiyeriab, R. FaghihMirzaeeb, K. Naviab and A. Momeniab. Design and analysis of a high-performance CNFET-based Full Adder. 2010.

[12] S. Shirinabadi-Farahani, R. Zarhoun, M. H. Moaiyeri and K. Navi. AN EFFICIENT CNTFET-BASED 7-INPUT MINORITY GATE. International Journal of VLSI design & Communicatio n Systems (VLSICS). pp. 4-1, 2013.

[13] S. A. Ebrahimi and P. Keshavarzian, S. Sorouri, M. Shahsavari. Low Power CNTFET-Based Ternary Full Adder Cell for Nanoelectronics. International Journal of Soft Computing and Engineering (IJSCE) ISSN. pp. 2231-2307, 2010.

[14] K. Navi, M. Rashtian, A. Khatir, P. Keshavarzian and O. Hashemipour. High Speed Capacitor-Inverter Based Carbon Nanotube Full Adder, Nanoscale Res Lett. pp. 859–862, 2010.

[15] JS. Hwang, HT. Kim, MH. Son, JH Oh, SW. Hwang, D. Ahn. Electronic transport properties of a single-wall carbon nanotube field effect transistor with deoxyribonucleic acid conjugation. Physica E: Lowdimensional Systems and Nanostructures. pp. 1115–1117, 2008.

[16] J. Guo, A. Javey, H. Dai, S. Datta, M. Lundstrom. Predicted performance advantages of carbon nanotube transistors with doped nanotubes source/drain. Phys Rev B Condens Matter. pp. 309-339, 2003.

[17] P. Keshavarzian and M. Mohammad Mirzaee. A Novel Efficient CNTFET Gödel Circuit Design. International Journal of Soft Computing and Engineering (IJSCE). pp. 296-300, 2012.

[18] P. Keshavarzian and M. Mohammad Mirzaee. A novel, efficient CNTFET Galois design as a basic ternary-valued logic field, Nanotechnology, Science and Applications. pp. 1–11, 2012.

[19] S. Farhana, A.H.M. ZahirulAlam and S. Khan. Development of a 2-Digit Multi Valued Analog-To-Digital Converter. World Applied Sciences Journal. pp. 622-625, 2012.

[20] S. Lin, Y. Kim and F. Lombardi. Design of a Ternary Memory cell Using CNTFETs. IEEE TRANSACTIONS ON NANOTECHNOLOGY. pp. 1019-1025, 2012.