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New CNFET- Based Full Adder cells for Low- Power and Low- Voltage Applications

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Abstract

Scaling challenges and limitations of conventional silicon transistors have led the designers to apply novel nano-technologies. One of the most promising and possible nano-technologies is CNT (Carbon Nanotube) based transistors. CNFET have emerged as the more practicable and promising alternative device compared to the other nanotechnologies. This technology has higher efficiency compared to the silicon-based MOSFET and is appropriate for high-frequency applications. Full Adder cell is the essential core and the building block of most arithmetic circuits and is placed on most parts of their critical paths .In this paper, power-efficient CNFET (Carbon Nanotube Field Effect Transistor) based Full Adder cell is proposed. This design is simulated in several supply voltages, frequencies and load capacitors using HSPICE circuit simulator. Considerable improvement is achieved in terms of power and PDP (Power-Delay-Product) in comparison with other classical CNFET-based designs, in the literature. Our proposed Full Adder can also drive large load capacitance and works properly in low supply voltages.

Keywords: *Full Adder, CNFET, High Speed, Low Power, Power Delay Product*

1. Introduction

Nanotechnology draws extremely attention from the researchers in recent years. MOSFET technology faces challenging problems, such as high power consumption and difficulties in feature size reduction. Due to these problems alternatives to conventional MOSFET technology being prospected. These contain the Quantum-dot Cellular Automata (QCA) [1], Carbon Nanotube Field Effect Transistor (CNFET) [2], and the Single Electron Transistor (SET) [3]. There are many similarities between CNFETs and MOSFETs in terms of intrinsic characteristics and operation. Therefore, in the nanotechnology era CNFET have emerged as the more practicable and promising alternative device compared to the other nanotechnologies. So there has been notable interest in the understanding and design of carbon nanotube field-effect transistors [4].

In general, CNFET has lower power consumption and higher efficiency compared to the silicon-based MOSFET and is appropriate for high-frequency and low-voltage applications. Another remarkable characteristic of CNFET is that P-CNFET and N-CNFET, with the same device geometries, consequently the same current drive capabilities, and have the same mobilities, which is very significant for transistor sizing in the intricate circuits. In recent years, several CNFET-based circuits such as Galois

field circuits, Multiple-valued logic circuits, and CNFET Full Adders have been proposed in the literature [4-6]. However, assuming all these structures, arithmetic circuits could be more of an interest on account of their extensive applications in the VLSI systems, such as micro/nano electronic systems, processors, and DSP architectures. As regards a Full Adder cell is the essential core and the building block of most arithmetic circuits and is placed on most parts of their critical paths, it has always been significant to design high-efficiency and high-speed Full Adder cells and as a result low Power-Delay Product (PDP) intricate arithmetic circuit [7-10].

In this paper low-PDP CNFET-based Full Adder is presented. The performance of the proposed design is evaluated in various situations and is compared to the other 32nm-CNFET Full Adder cells of different styles. In the reminder of this paper, in section 2 a brief review of the CNFET technology is presented. In the next section related work on designing a full adder cell is discussed. The proposed CNFET-based Full Adder cell is presented in section 4. The experimental results, analyses and comparisons are presented in section 5 and finally, section 6 concludes the paper.

2. Brief Review of Carbon Nanotube Field Effect Transistors (CNFETs)

Carbon Nano tubes are hollow pipes made of carbon sources such as graphite with naphthalene or gas, and etc. [4]. CNTs can be classified into single-walled CNTs (SWCNTs), made up of a single tube, and multi walled CNTs (MWCNTs), made up of more than one tube. For each tube a vector named chirality vector, which is identically the wrapping vector that the graphite sheet is considered to be rolled up along it. The chirality vector establishes the constitution angle of the carbon atoms along the nanotube. It is explained by (n,m) pair named chiral numbers and represented many electrical and physical properties of the CNT. A SWCNT is a semiconductor if $n - m \neq 3k$ ($k \in Z$), otherwise it is a conductor [9, 11, 12].

The threshold voltage of the carbon nano tube channel is depended to its diameter [11], Equ. 1.

$$V_{th} = \frac{\sqrt{3}}{3}\frac{aV_{\pi}}{eD_{CNT}} \tag{1}$$

Where e is the unit electron charge, $V\pi = 0.033$ eV is the carbon π-π bond energy, a = 2.49 Å (angstrom) is the carbon to carbon atom distance, and D_{CNT} is the CNT diameter, as indicated in Equ. 2.

$$D_{CNT} = \frac{\alpha\sqrt{3}}{\pi}\sqrt{n^2 + m^2 + nm} \tag{2}$$

In Equ. 2, n and m are chirality of CNT and $\alpha = 0.142nm$ is the inter-atomic distance between each carbon atom and its neighbor. As illustrated in Equ. 1, the threshold voltage of CNFETs depends to the opposite of the diameter of nanotube used as a channel. As a result, different transistors with different turn on voltage can be implemented by changing the diameter of CNT [12].

3. CNFET Full Adder Cells in the Literature

Many full adder cells have previously been presented in the literature. Some of full

adders have been constructed with three inputs *NAND, NOR*, or *Majority-NOT* functions [4, 9, 12-19] . These functions can be obtained by setting threshold voltage of the inverter displayed by Fig. 1 to an appropriate value. In this figure the size of capacitors is equal C which can be picked by the circuit designer to gain the best efficiency. Accordingly, these adders benefit from simple construction and reduced number of transistors.

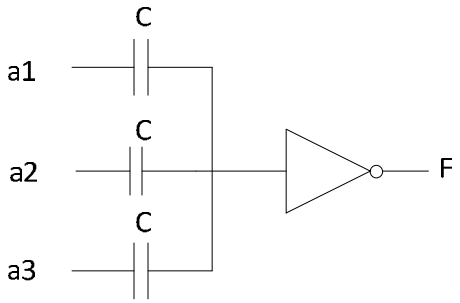

Fig. 1. NOR, NAND and Majority-NOT functions.

In the followings some of CNFET full adder cells are discussed. The design in [13], is based on three-input *Majority-NOT, NAND* and *NOR* functions. A *Majority-NOT* function is utilized to construct $\overline{COUT}$ and another one together with two *NAND* and *NOR* gates are used for creating *SUM* output based on Equ. 3 and 4. This design is composed of 8 capacitors and 8 transistors.

$$\overline{COUT} = \overline{Majority(A,B,C)} = \overline{AB + AC + BC} \tag{3}$$

$$SUM = \overline{Majority(A,B,C,2NAND(A,B,C),2NOR(A,B,C))} \tag{4}$$

In another full adder cell [14], $COUT$ output is produced in similar method in which a four-input *Majority-NOT* function is used in order to creat $\overline{SUM}$, based on Equ. 5.

$$SUM = Majority(A,B,C,\overline{COUT},\overline{COUT}) \tag{5}$$

The design in [15], is modified version of full adder circuit in [14]. This design reduces the number of capacitors and uses 8 transistors. This approach improves the energy performance and speed and increase the efficiency of the cell.
The *SUM* output in the other full adder, is included of two parts. part 1, composes three capacitor which calculates scaled weighted sum of input signals. Part 2 composes CNT transistor with different threshold voltage to generate full adder outputs. This design is a multi-output structure [17].

Another threshold logic full adder is designed in [16]. In this way of designing circuit, the output is equal to logic '0' if the weighted sum of the input values is lower than the threshold value, T , otherwise it is equal to logic '1'. In fact, the output of a threshold logic gate is determined by Equ. 6. In this equation the set of input variables and weights are defined by $\{x_0, x_1, ..., x_{n-1}\}$ and $\{w_0, w_1, ..., w_{n-1}\}$, respectively [20]. The CNFET implementation of this full adder cell consistent with the related Equ. 6-10 is created with the structure of Fig. 1. In the first phase, three threshold gates are used to produce $COUT, NAND(a,b,c)$ and $NOR(a,b,c)$ gates. In the next phase, another threshold

gate is fed to these gates to create *SUM* output.

$$F(X) = Sign\{F(X)\} = \begin{cases} 0, if\ ..F(X) < 0 \\ 1, otherwise \end{cases}$$
$$F(X) = \sum_{i=0}^{n-1} w_i x_i - T \quad (6)$$

$$NOR(a,b,c) = \overline{sign(a+b+c-1)} \quad (7)$$

$$NAND(a,b,c) = \overline{sign(a+b+c-3)} \quad (8)$$

$$COUT = sign(a+b+c-2) \quad (9)$$

$$SUM = sign(NOR(a,b,c) + NAND(a,b,c) + COUT - 2) \quad (10)$$

An energy-efficient symmetric full adder cell is designd in [18] (Fig. 2a). The SUM and COUT output is generated in a unit structure and this signals are produced concurrently. In this full adder cell, inverter of input signals are generated using shared transistors. this process leads to elimination of six transistor. The SUM and COUT signals of full adder cell in [19] (Fig. 2b) are generated separately in parallel maner. This cell has 18 transistors. The full adder cell [9] shown in Fig. 2c is according to three input NAND, NOR, and minority functions. It is composed of 3 capacitors and 14 transistors.

4. Proposed Designs

In this section two novel fast full adder cells based on CNFET are presented.The proposed full adder cells are composed of two types of circuits: XOR-XNOR circuits and multiplexers (MUX). Pass transistor uses to implement a given function. Pass transistor logic reduces the count of transistors used to make different functions, by removing redundant transistors. This method leads to reduce the power, delay, and the number of transistors. In the First step, pass-gates are used in order to realize *XOR* (a,b) and *XNOR* (a,b) functions. This structure is presented in Fig. 3.

In Fig. 3 When 'B=0', then the transistors T1 and T3 are 'ON'. In this circumstance, *OUT1* output is equal to 'a', and *OUT2* output is equal to '$\bar{a}$'.On the other hand, when 'B=1', then the transistors T2 and T4 are 'ON'; and as a result, *OUT1* output is equal to '$\bar{a}$', and OUT2 output is equal to 'a'. So, *OUT1* output is equivalent to $a \otimes b$, Equ. 11; and *OUT2* output is equivalent to $\overline{a \otimes b}$, Equ. 12.

$$a \otimes b = a.\bar{b} + \bar{a}.b \quad (11)$$

$$\overline{a \otimes b} = \bar{a}.\bar{b} + a.b \quad (12)$$

Based on Equ. 13, *SUM* of a full adder is the output of a multiplexer. In this multiplexer, 'c' input is considered as its switch control, and *XOR, XNOR* sub-module is considered as its data inputs.

$$SUM = (a \otimes b).\bar{c} + \overline{(a \otimes b)}.c = (\bar{a}.b + a.\bar{b}).c + (\bar{a}.\bar{b} + a.b).\bar{c} = \bar{a}.b.c + a.\bar{b}.c + a.b.\bar{c} + a.b.c \quad (13)$$

A. First Proposed Design of full adder cell

Different combinations of *XOR/XNOR* gates and multiplexer blocks can be used to implement a full adder circuit.We have used two XOR/XNOR cells and a pass ransistor multiplexer to design a full adder, as shown in block diagram of Fig. 4.

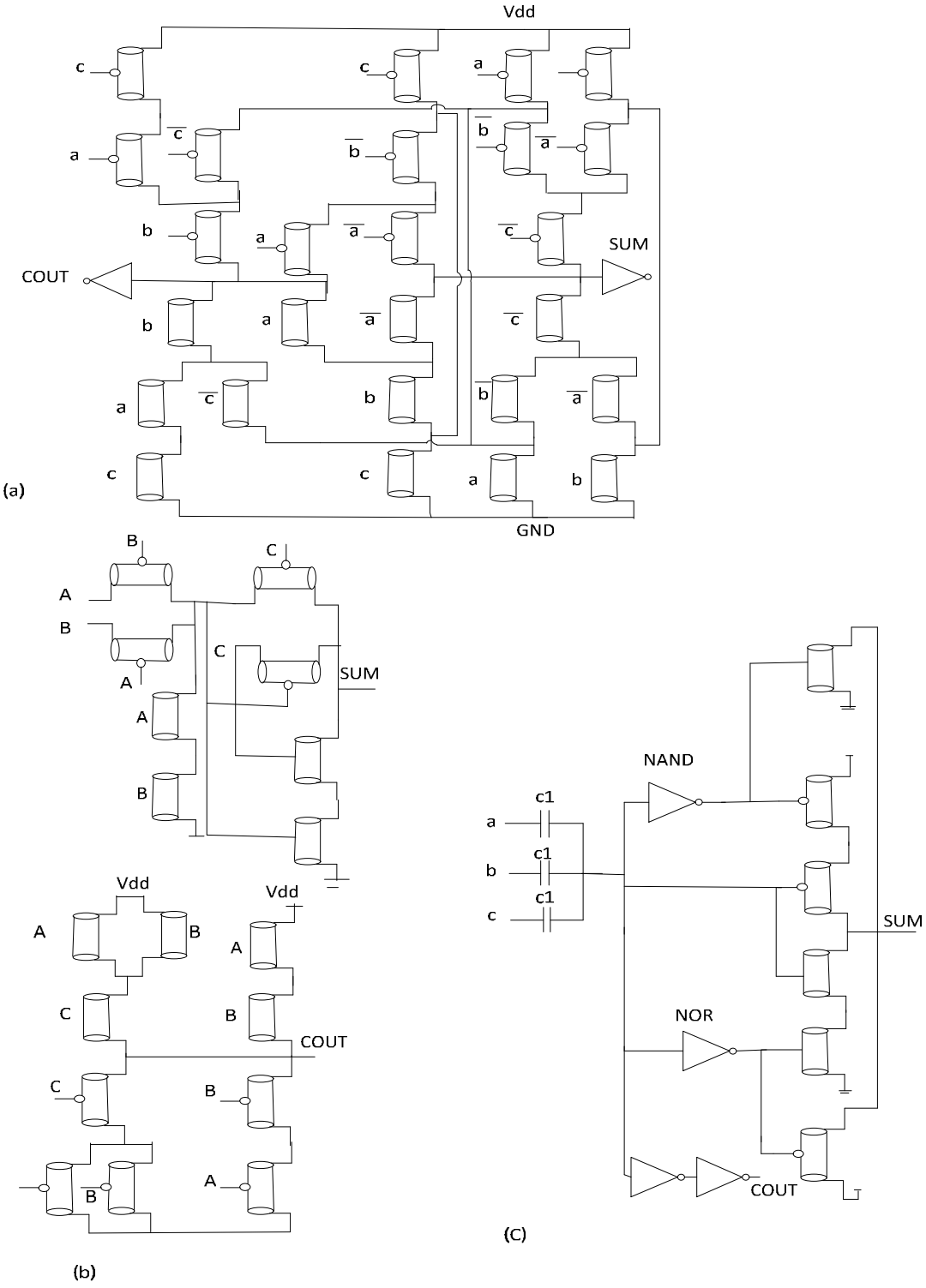

Fig. 2. Full adder designs. (a) design in [18], (b) design in [19], (c) design in [9]

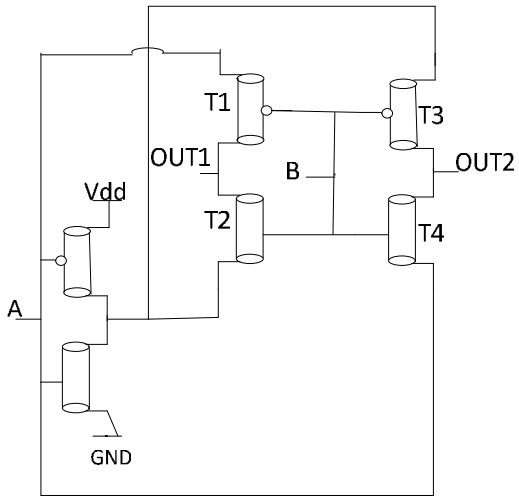

Fig. 3. XOR and XNOR functions.

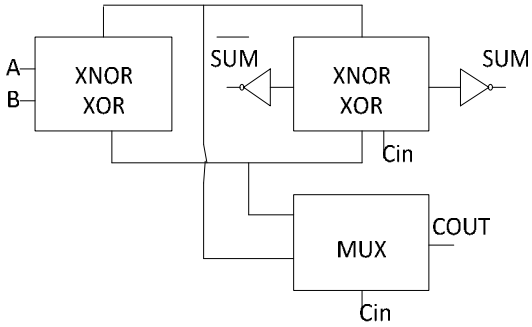

Fig. 4. Block diagram of the first proposed full adder.

In this design, *SUM* output is constructed in two stages. First, structures of Fig. 3 are exploited for realizing *XOR* (a, b) and *XNOR* (a, b) functions. Afterward, in the second stage, the same structure is produced the SUM and $\overline{SUM}$ outputs of full adder cell, simultaneity, Equ. 13. Figure 5 shows the first proposed full adder cell.

For designing *COUT* output similar to the mentioned method, , a 2-to-1 multiplexer is used Equ. 14. The selector in this multiplexer is '$(a \otimes b)$', and its two inputs are '*c*' and '*a*'.

$$COUT = (a \otimes b).c + \overline{(a \otimes b)}.a = (\bar{a}.b + a.\bar{b}).c + (\bar{a}.\bar{b} + a.b).a = a.b + \bar{a}.b.c + a.\bar{b}.c = a.b + a.c + b.c \quad (14)$$

B. Second Proposed Design of full adder cell

The *SUM* output in the second full adder design is also builds in two stages. The first stage is similar to prior design. Next, $\overline{SUM}$ is produced through a 2-to-1 multiplexer. It controls with $(a \otimes b), \overline{(a \otimes b)}$, (Fig. 6). Then, $\overline{SUM}$ output is inverted to produce *SUM* output. The *COUT* output in this structure is produced similar to prior design. It can be inferred from the waveforms of simulation. These designs act very well at low supply voltages and they give full swing outputs.

5. Simulation Result

In this section, for exploring the performance of proposed cell, comprehensive simulations have been presented. The simulation results compared to the same CNFET

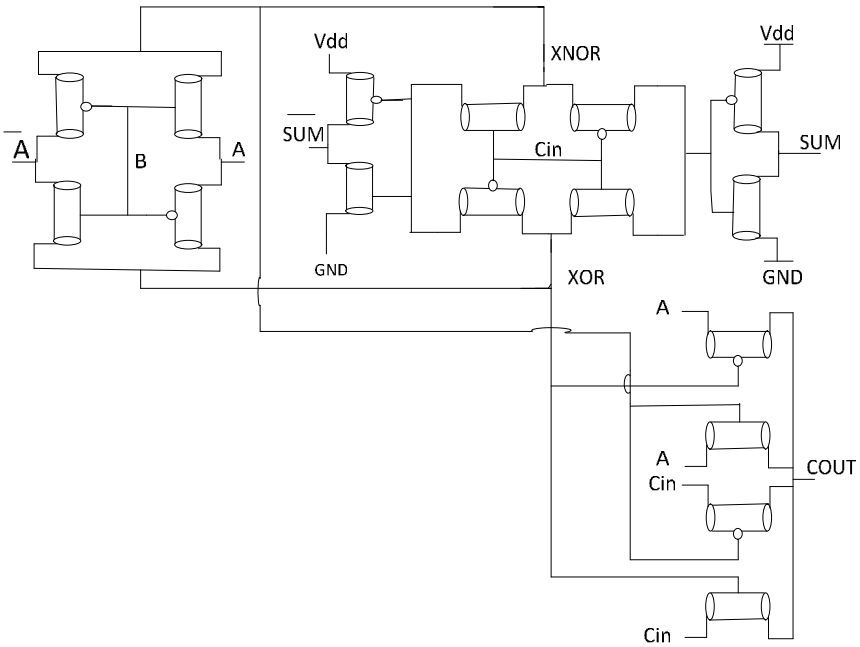

Fig. 5. CNFET circuit of the first proposed full adder.

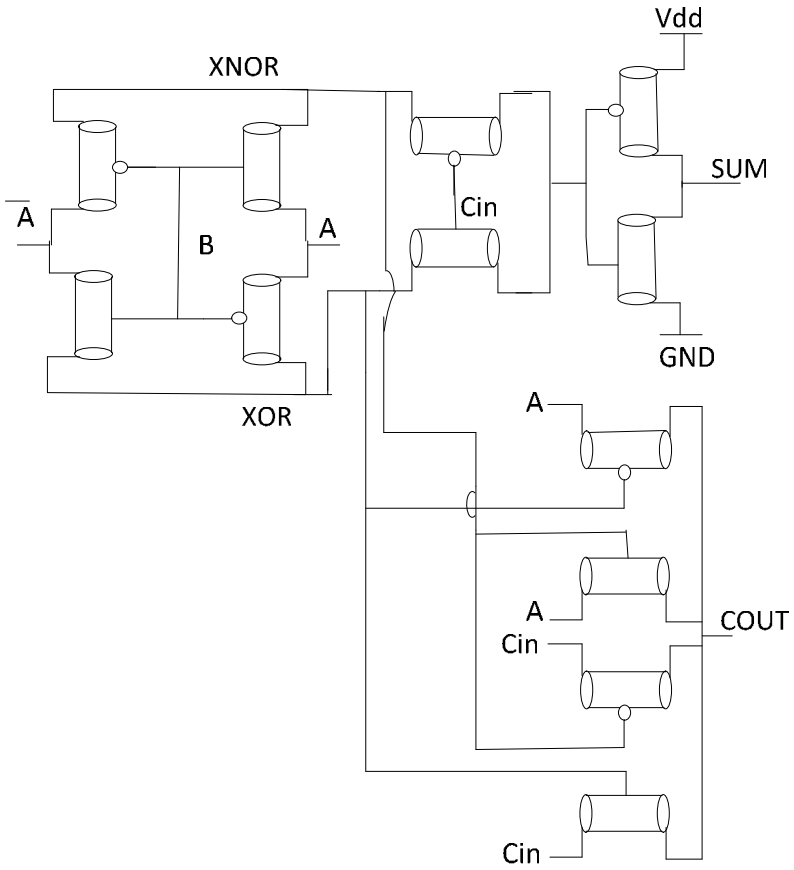

Fig. 6. CNTFET circuit of the second proposed full adder.

based cells. For these simulations , Synopsys HSPICE 2008 simulator and compact SPICE model have been used which is more described in[21, 22]. In these comparisons, 32nm Predictive Technology Model (PTM) has been used which designed for unipolar,

MOSFET-like CNFET devices for the transistors which have one or more CNTs. This CNFET model also takes into account SB effects, parasitic, including CNT, source/drain, and capacitances and gate resistances and CNT charge screening effects. The model also contains a full trans capacitance network for more careful dynamic and transient performance simulations.

The designs are optimized in terms of ,Delay, Power consumption, and PDP. The delay of each cell is computed from the 1/2 Vdd to the time that the output signal reches the same level of Vdd. All possible input transitions from an input to another are checked and the maximum delay has been reported as the delay of each circuit. The average power consumption during a long period of time has been considered the power consumption metric. In each circuit the number of tubes has been changed to achieve the best PDP (Power Delay Product). For thorough evaluation of functionality of the designs in different conditions. Simulations are performed in different output loads, frequencies, supply voltages, and room temperatures. The proposed designs have been simulated at room temperature at 0.6, 0.8, and 0.9 V supply voltages, and all at operating frequencies equal to 100 MHz and 250 MHZ, and different load capacitance.

First, the circuits are simulated at 0.6 V , 0.8V and 0.9 V supply voltages and at 100 MHz operating frequency with 2.1fF output load capacitance. The results of this simulation are shown in Table 1. According to the experimental results, proposed designs have the lowest power and PDP compared to the other designs at all supply voltages.

In the second experiment, all the circuits are simulated at the three mentioned supply voltages and 250 MHz frequency using 2.1fF output capacitor. The results are shown in Table 2.The proposed designs have the best PDP and power consumption in comparison with other circuits at all supply voltages.

Table 1. The first simulation results of delay, power, PDP (f=100 MHZ, Cload=2.1 fF)

Vdd (V)	0.6	0.8	0.9
Delay $(\times 10^{-12} s)$			
CNT- Design in [18]	134.23	68.211	55.705
CNT- Design in [19]	110.97	45.529	34.726
CNT- Design in [9]	67.067	81.501	47.995
Proposed Design	126.692	52.920	42.326
Average power $(\times 10^{-6} w)$			
CNT- Design in [18]	4.1450	10.910	15.990
CNT- Design in [19]	0.09309	0.1680	0.2146
CNT- Design in [9]	0.3146	0.1895	1.7595
Proposed Design	0.06184	0.1176	0.1520
PDP $(\times 10^{-17} j)$			
CNT- Design in [18]	55.637	74.420	89.075
CNT- Design in [19]	1.0330	0.7650	0.74538
CNT- Design in [9]	2.1100	1.5446	8.4447
Proposed Design	0.7849	0.6226	0.6435

Simulation results for different capacitance load of 1fF to 8fF at 100 MHZ frequency and supply voltage of 0.6V are shown in Table 3. As it is seen in this table, the PDP of the proposed adder is less than other exiting adders. Another important characteristic of the circuits which should be considered is their inviolability to the ambient temperature variations. Thus, for investigating their sensitivity to temperature variation and noises, the proposed circuits are simulated in a vast range of temperatures, from $0^{o}C$ to $80^{o}C$ at

0.6V supply voltage and 100 MHz operating frequency with 2.1fF output load capacitance. The results are plotted in Table 4. It can be seen from this table that the proposed designs have a normal functionality.

Table 2. The second simulation results of delay, power, PDP (f=25oMHZ, Cload=2.1fF)

Vdd (V)	0.6	0.8	0.9
Delay $(\times 10^{-12} s)$			
CNT- Design in [18]	23.516	16.152	14.474
CNT- Design in [19]	99.244	41.797	32.679
CNT- Design in [9]	81.661	48.768	43.402
Proposed Design	125.14	52.706	42.258
Average Power $(\times 10^{-6} w)$			
CNT- Design in [18]	4.5835	12.015	17.602
CNT- Design in [19]	0.2377	0.4255	0.5434
CNT- Design in [9]	0.3458	2.1618	4.7136
Proposed Design	0.1400	0.2713	0.3536
PDP $(\times 10^{-17} j)$			
CNT- Design in [18]	10.77	19.407	25.477
CNT- Design in [19]	23.590	17.787	17.760
CNT- Design in [9]	2.8246	10.543	20.458
Proposed Design	1.7529	1.4301	1.4945

In addition, in order to evaluate the Full Adders as a building block of larger structures, eight cells of the proposed Full Adder are cascaded and simulated at 0.65V supply voltage as shown in Fig. 7.The delay, power consumption and PDP of this structure are 1000.6 ps, 3.2914 mW and 32.932 aJ, respectively. these parameters for other a design using the cell presented in [11] are 42.7ps, 0.41mW and 174 aJ, respectively. The results show that the proposed design can also operate with high performance in the larger structures.

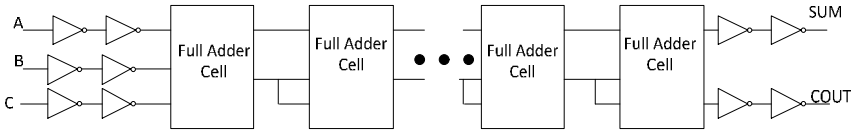

Fig. 7. Eight cascaded proposed cells.

The effect of process variation is the last effort to check the efficiency of proposed design. Process variation is a significant concern in nano ranges characteristic size and can negatively affect the efficiency of the circuits. Since a CNFET is more sensitive to diameter variation than width and length variations, the diameter variation of CNTs is the most considerable parameter. Monte Carlo transient analysis with a logical number of 30 iterations for each simulation is carried out to measure the sensitivity of the proposed designs to process variations. The simulation is repeated 10 times and the largest deviation is saved as the result. The statistical significance of 30 iterations is very high. If a circuit operates accurately for all 30 iterations, there is a 99% prospect that over 80% of all of the feasible component values it operates perfectly. Distribution of the diameter is considered as Gaussian with 6-sigma distribution which is a sensible for assumption large numbers of fabricated CNTs.

Additionally, a standard derivation of 0.04 nm to 0.2nm is mistaken into attention for

each mean diameter value. The experimental results are presented in Table 5.This test indicates that the lowest variation of the proposed circuit in term of delay, power and power-delay product in comparison with previous works.

Table 3. PDP versus output load capacior (suply voltage=0.6 V, frequency=100MHZ)

Load Capacitor (fF)	Design in [18]	Design in [9]	Proposed design	Design in [19]
1	3.68E-16	6.22E-18	1.94E-18	3.34E-18
2	5.41E-16	1.43E-17	7.13E-18	9.00E-18
3	6.95E-16	2.58E-17	1.54E-17	1.70E-17
4	8.35E-16	4.04E-17	2.66E-17	2.68E-17
5	9.73E-16	5.80E-17	4.11E-17	3.87E-17
6	1.11E-15	7.87E-17	5.73E-17	5.23E-17
7	1.24E-15	1.03E-16	7.70E-17	6.75E-17
8	1.36E-15	1.30E-16	1.00E-16	8.51E-17

Table 4. PDP versus temperature (supply voltage=0.6 V, frequency= 100MHZ)

Temperature (^0C)	Design in [18]	Design in [9]	Proposed design	Design in [19]
0	7.0704E-16	1.2838E-17	8.7432E-18	1.1925E-17
10	7.0704E-16	1.3671E-17	8.3445E-18	1.1010E-17
20	5.4338E-16	1.4680E-17	7.9404E-18	1.0186E-17
30	5.4338E-16	1.5794E-17	7.7906E-18	9.5169E-18
40	5.0575E-16	1.7030E-17	7.5190E-18	8.9317E-18
50	4.6881E-16	1.8625E-17	7.3262E-18	8.4620E-18
60	4.4043E-16	2.0406E-17	7.1355E-18	8.0258E-18
70	4.1387E-16	2.2316E-17	7.0260E-18	7.6557E-18
80	3.9146E-16	2.4313E-17	6.8553E-18	7.3150E-18

Table 5. Process variation of full adder cells.

D-VAR	.04	.06	.08	0.1	0.12	0.16
PDP-VAR ($*10^{-17}$)						
Design in [14]	0.141	0.291	0.443	0.499	0.473	0.698
Design in [15]	0.494	0.772	1.085	1.46	1.92	3.387
Design in [16]	0.07	0.17	0.238	0.35	0.472	0.767
Proposed-FA	0.544	.0801	.1022	0.1255	01496	0.1933
Delay-Var($*10^{-11}$)						
Design in [14]	1.042	1.569	2.069	2.646	3.291	5.25
Design in [15]	0.537	0.785	1.081	1.469	1.972	3.653
Design in [16]	0.466	1.025	1.466	2.138	2.792	4.402
Proposed-FA	0.0054	1.519	1.98	2.41	2.89	3.746
Power-Var($*10^{-7}$)						
Design in [14]	0.235	0.351	0.464	0.59	0.721	1.987
Design in [15]	0.73	1.124	1.514	1.918	2.344	3.228
Design in [16]	0.132	0.188	0.246	0.302	0.381	0.327
Proposed-FA	0.0544	.0089	0.0104	0.0139	0.016	0.0231
Design in [14]	0.235	0.351	0.464	0.59	0.721	1.987

6. CONCLUSION

In this paper two low-voltage CNFET-based Full Adder circuits for nanotechnology are proposed. Carbon nanotubes have emerged as the most promising alternative device and there has been notable interest in the understanding and design of carbon nanotube field-effect transistors. Full Adder cell is the essential core and the building block of most arithmetic circuits. Proposed designs have rail-to-rail output signals and work properly at low voltages. In order to evaluate its performance some conventional and state-of-the-art 32nm CMOS and CNFET-based full Adder designs are simulated. The simulation results indicate that significant improvement in terms of energy and efficiency and PDP are achievable in different test conditions by utilizing the proposed circuits.

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