Reducing the Consumption Power in Flash ADC Using 65nm CMOS Technology

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Abstract

This paper presents a new method to reduce consumption power in flash ADC in 65nm CMOS technology. This method indicates a considerable reduction in consumption power, by removing comparators memories. The simulations used a frequency of 1 GHZ, resulting in decreased consumption power by approximately 90% for different processing corners. In addition, in this paper the proposed method was designed using interpolation technique for purpose of promoting the performance as well as decreasing the class of chip. The simulation results indicate that the consumption power for interpolation technique was decreased by approximately 5% compared to the proposed method. Also, we compare the results of the proposed technique with those of convertors frequently referred in other studies. The results show that the consumption power is considerably decreased, using the proposed technique.

Keywords: flash ADC, consumption power, 65nm CMOS technology

1. Introduction

Today, most data is characterized by analog signals. In order to manipulate the data using a microprocessor, we need to convert the analog signals to the digital signals. Using CMOS technology due to the potential of high integration, low consumption power and low cost method to build a conventional analog-to-digital converters (ADC, or A/D) is presented. An analog-to-digital converter is an electric circuit that converts an analog voltage into its digital representation. Today, designing ADC is emphasized given the extensive use of convertors in telecommunication, electronics, and control systems. The advantages have inspired the researchers and manufactures to use integrated circuits (IC) in making and developing convertors. It is noteworthy that the parallel comparator type (flash) ADCs is mainly used for high speed and low resolution applications [1-3].

The quality of converter is combination of speed, number of bit and consumption power. However, in many cases, consumption power by itself is an indicator of the quality. Encouraged by the extensive use of data convertors in widely used systems such as telecommunication systems, videos, television, wireless systems, the researchers have sought to decrease the consumption power so that the use of a convertor with high speed and low consumption power has turned into a research focus. As an ADC and because of its high speed and simple circuit, flash convertor is commonly used in industry. Due to their high speed, simple circuit and parallel processing capability, flash convertors are preferred over other types even the former are less accurate. However, reducing the consumption power is the main challenge faced by the researchers. This study presents an applied method aiming at reducing the consumption power in flash ADC. Figure 1 shows a conventional *N* bits flash ADC in the general case. As figure1 shows, flash convertor consists of three main components: resistor string, comparator, and encoder. The number of resistor strings is and the number of comparators is -1 for Bit output. In flash convertor, the comparisons conducted by comparator are transmitted to thermometer to binary code convertor and converted into a binary code. Also (-1) encoder converts its input thermometer code to bit binary code. Initially, the comparator compares the input voltage) against the reference voltage ,), where$= 1, 2, \ldots, 2^N - 1$, on resistor ladder. Then, the comparison results ,) are transmitted to thermometer to binary code convertor. The

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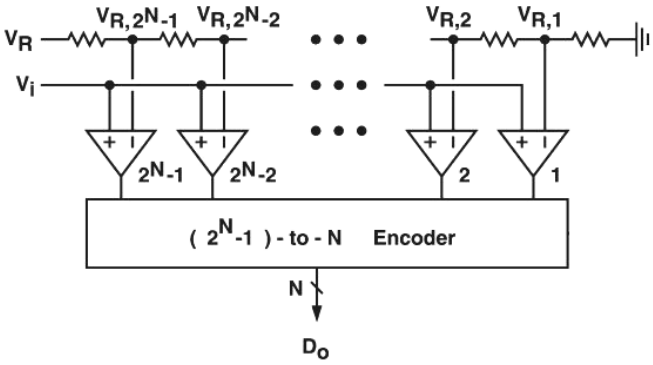

Fig. 1. Conventional flash ADC architecture [4].

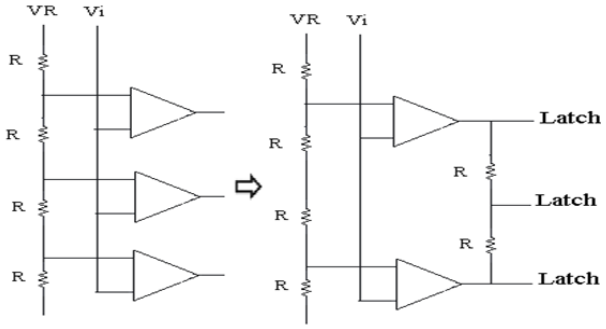

Fig. 2. Interpolation technique [1, 2].

downsides of this circuit include kick back noise, bubble error, large size of hardware and high consumption power. The kick back noise and bubble error are removed by inserting pre amplifier and AND-OR logical gates in the circuit respectively.

The circuit interpolation technique can be used to reduce the size of hardware. Recently, interpolation has been widely used to reduce the consumption power and chip class and hence the costs. The proposed method draws on interpolation for purpose of reducing the hardware size and consumption power. Figure 2 shows how this technique is implemented. For example, in an bit flash convertor, there will be -1 comparators, which will be reduced, based on circuit distortion technique which works as follows: It uses alternately the resistance voltage division instead of preamplifier. Due to its high speed, accuracy and low size as well as its simplicity of circuit, this technique is very important [1-6].

The rest of this paper is organized as follows. Section 2 describes the proposed method. Section 3 will present the simulation results yielded by the proposed method and interpolation technique. Finally, some conclusions are provided in section 4.

2. Proposed Method

The increasing demand for integration of data convertor circuit as well as the increased application of convertors in electronic devices and the industries such as medical science, telecommunication and military have brought the researchers and users' attention to the necessity of reduction in consumption power. The recent years have seen the rapid development of ADC hardware as well as digital signals processing. The consumption power indicates the extent to which power is used in various blocks of a circuit. The consumption of more power leads to both higher price and a decrease in circuit life cycle. This study aims to offer a method to reduce the cost and consumption power as well to increase the life cycle of the convertor [7-14].

Generally, the consumption power is divided into two categories: 1- dynamic, 2- static. One of the main causes of consumed power in CMOS circuits is due to the charging and discharging of the node capacitances of the circuits, present both as a load and as parasitic. Such part of the total consumed power is called dynamic power. In addition, the static power results from the consumed power due to charge injection and the consumed power by voltage source. Literature on convertors shows the role of convertors calibration in reducing the consumption power. This is achieved by reduction in comparators offset through the proper design of transistors [1, 2]. Memory block is a component of comparator circuit which holds and transmits the data to the output. The proposed technique by this study decreases the consumption power with removing comparators memories and calibration. Figure 3 shows how memory is removed from comparator. A logical procedure is used to meet the goal and to control the timing of the circuit, thereby its duty namely the maintaining and transmitting the data to the output is performed, followed by the arrival of the next clock.

Flash convertor has a high speed which in turn depends on the comparator speed. The comparators are made, using the technology of integrated circuits. However, the speed of integrated circuits depends on transistors dimensions. Therefore, transistors dimensions influence the speed of comparators which, in turn influence the speed of flash convertor. The 65nm CMOS technology used in the proposed method decreases the dimensions on transistor scale. This increases the speed of integrated circuits performance, leading to decreased consumption power by decreasing the dimensions and advanced technology. Input signal in flash convertors is periodic, continuous and changing and is added to the circuit in a given time range step by step for purpose of properly being processed. A sample and hold circuit based on charge injection is used at the beginning of the circuit for achieving proper timing and sampling improvement. This solves the clock feed through and charge injection problems. As a result the consumed power due to leakage current is reduced. Being a comparator, XNOR gate is used to ensure the reliability of comparators output results. This gate is selected among other gates because of its performance at the time when the outputs of both comparators are equal. If both inputs of this gate are equal, the output would be ' amount which is

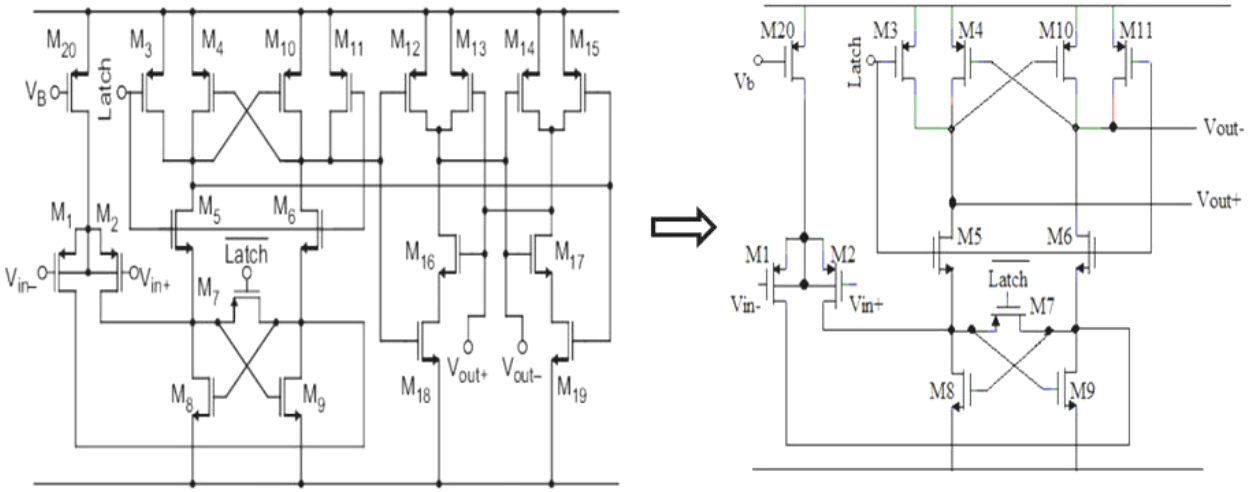

Fig. 3. Resizing comparator circuit [7].

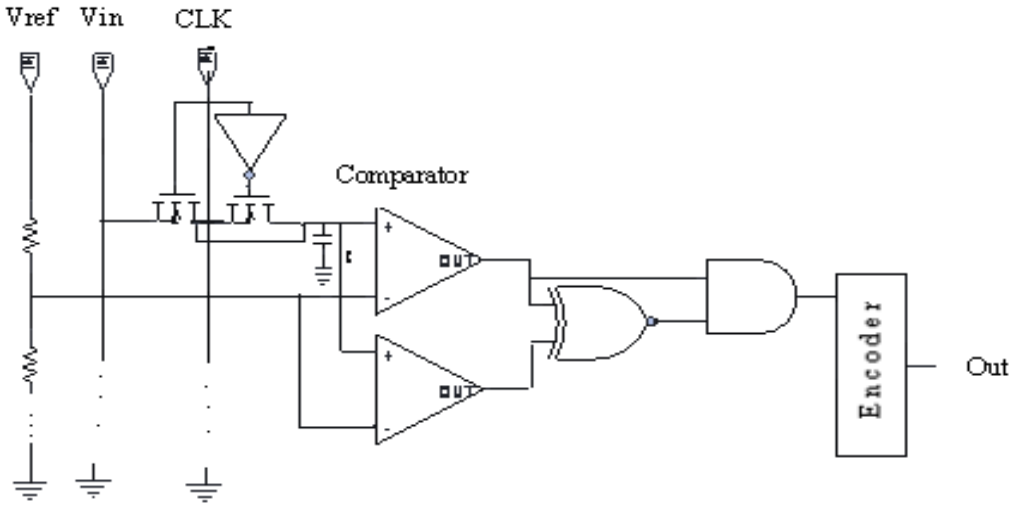

Fig. 4. A class of proposed flash ADC.

compatible with comparators performance. Moreover, AND gate is used to increase the reliability of the proposed circuit. Figure 4 shows a level of the circuit designed on the basis of above-mentioned description.

The performance of the proposed circuit at the time when input signal is to be sampled is as follows: comparator compares the voltage obtained from the sample with its reference voltage. The results of both comparisons are applied to XNOR gate for purpose of ensuring the reliability of the results. The AND logical gate is also used to meet the duty of memory followed by the arrival of next clock. This process also reduces the consumption power and increases the reliability of the system. The interpolation technique is used to decrease the class of chip as well as prices (see figure 5).

The performance of this circuit is similar to that of circuit in figure 4. But in the former the comparator is removed alternately and the resistor voltage division is used to meet the circuit performance. This decreases the class of chip and hence the price of circuit designs.

3. Simulation Results

This section deals with the performance of proposed method and interpolated circuit and compares it with the commonly used method. The simulations were conducted using flash ADC with a 3 bit accuracy and sampling frequency of 1 GHZ in 65nm CMOS technology. The following section compares the proposed convertor with those designed in [15-17].

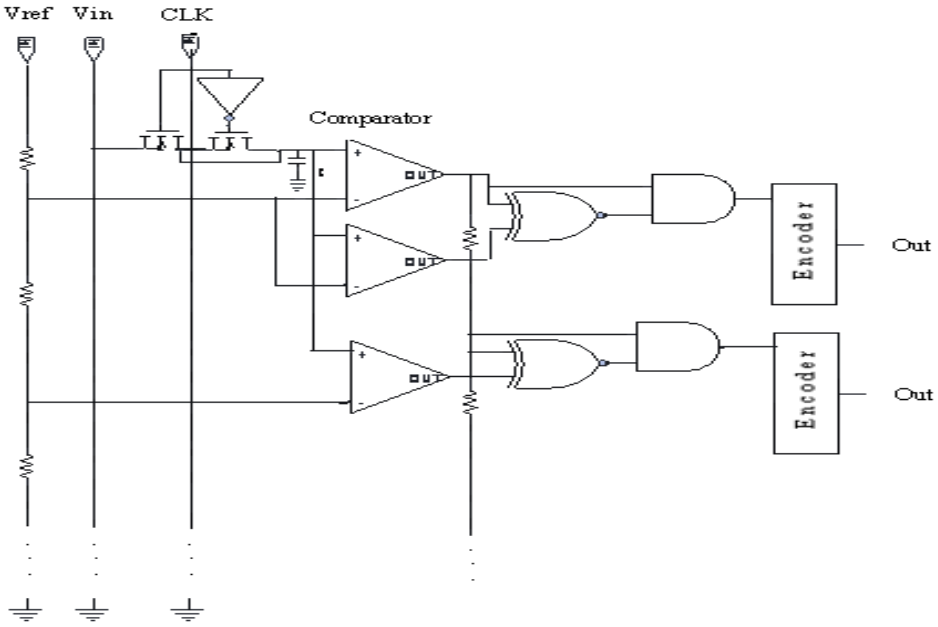

Fig. 5. A class of proposed flash ADC using the interpolation technique.

In semiconductor manufacturing, a process corner is an example of a design-of-experiments (DoE) technique that refers to a variation of fabrication parameters used in applying an integrated circuit design to a semiconductor wafer. Process corners represent the extremes of these parameter variations within which a circuit that has been etched onto the wafer must function correctly. In this paper, we compare the results of the proposed method with the other convertors for three processing corners: typical-typical (TT), fast-fast (FF), and slow-slow (SS).

Table 1 shows the simulations results for the proposed method and circuit interpolation in comparison with the conventional method for various processing corners and different temperatures. As the table1 shows, the consumption power is reduced to 16.81mW, using the proposed method for the TT corner and temperature . This indicates a decrease in consumption power by approximately 153mW in comparison with the conventional method. It can be also observed that the consumption power using the interpolation technique is lower than that with the proposed method. On the other hands, table 1 shows, the use of the proposed method and interpolation technique lowers the consumption power by approximately 148mW and 150mW for SS corner and temperature , respectively in comparison with the conventional method. In addition, compared to the conventional method, the consumption power will be lowered to by approximately 138mW and 141mW for FF corner and temperature , using the proposed method and interpolation technique, respectively. Also, table 1 shows that using the proposed method at the TT corner and temperature leads to more reduction in the consumption power than the reduction obtained for other corners. This had been predicted given the transistors switching in good conditions.

The maximum reduction in consumption power at the TT corner in comparison with the conventional method indicates that the effective number of bit has approached the nominal 3 Bit, indicating the decreased figures of merit (FOM), using the proposed method. It should be mentioned that the FOM is one of the main criterions for selection of convertor. This criterion indicates the extent to which the system performance as well as electronic components catch up with technology advancement. The lesser the consumption power, lower FOM. The FOM is calculated as follows [1]:

$$FOM = \frac{Total\ Power}{f_s \times 2^N} \quad (1)$$

In equation (1), is Bits and is sampling frequency of the convertor. It is worth mentioning that in this paper, *N* is 3 bits and is 1GHZ for proposed method.

Comparing the proposed methods with the conventional method, table 2 shows the FOM for different processing corners. According to this table, by using the proposed method and convertor interpolation, the FOM has been improved compared to the conventional method. It can also be seen that the FOM in the proposed converter with interpolation technique is lower than that in the proposed method. On the other hand, we observe that the FOM is reduced maximally at the TT corner in comparison with the other processing corners. Also, figure 6 shows the FOM for the proposed method, convertor interpolation, and conventional method at three processing corners.

Table 1

The consumption power for the proposed converters and conventional method at different processing corners

Converter	Consumption Power for FF Corner and Temperature	Consumption Power for SS Corner and Temperature	Consumption Power for TT Corner and Temperature
Conventional Converter	155.3mW	164.6mW	170mW
Proposed Converter	17.19mW	16.07mW	16.81mW
Proposed Converter with Interpolation Technique	14.17mW	13.78mW	13.81mW

Table 2

The FOM for the proposed methods and the conventional method at different processing corners

Converter	FOM for FF Corner and Temperature	FOM for SS Corner and Temperature	FOM for TT Corner and Temperature
Conventional Converter	21.250^{-15}	20.570^{-15}	19.410^{-15}
Proposed Converter	2.100^{-15}	20^{-15}	2.140^{-15}
Proposed Converter with Interpolation Technique	1.720^{-15}	1.720^{-15}	1.770^{-15}

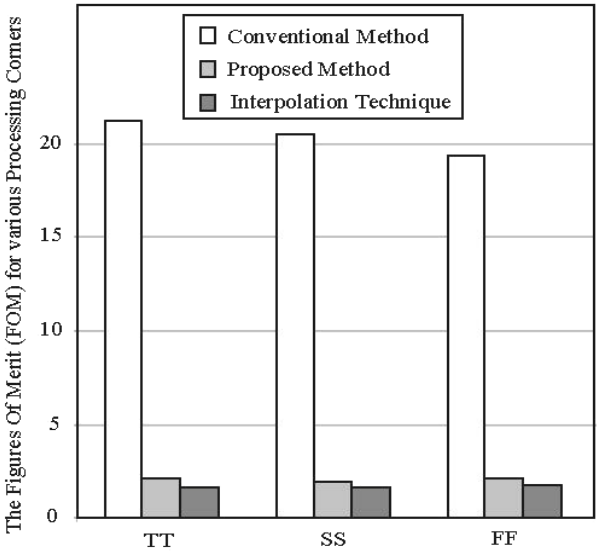

Fig. 6. The FOM for the proposed methods and the conventional method at three processing corners.

Finally, table 3 presents the consumption power for the proposed method in comparison with the other methods in references [15-17]. It should be mentioned that in this table, we compare the technology and the power consumption, combined with the expression of converter quality factors including speed, number of bit and consumption power. Accordingly, this table shows that the extent to which the consumption power in the proposed method is reduced depends on the accuracy, speed and the type of the technology used.

Table 3

Comparing the proposed convertor with the proposed convertor in references [15-17]

Converter	Frequency	TSMC	Bit	Consumption Power in TT Corner
Reference [15]	20 MHZ	0.18μm	3	36.273 mW
Reference [16]	20 GHZ	65nm	3	5.1W
Reference [17]	1 GHZ	90nm	6	72 mW
Proposed Method	1 GHZ	65nm	3	16.81mW

4. Conclusions

In this paper, we proposed a new method for reducing the consumption power in 3 Bit ADC in 65nm CMOS technology. It has been shown that the consumption power is much lower, using the proposed method in comparison with the conventional method. Moreover, convertor interpolation method was used to improve the performance of proposed convertor, resulting in the reduced consumption power of the convertor. On the other hand, it has been shown that the consumption power for the TT corner is decreased in comparison with that the SS and FF corners. It has also been observed that the FOM in proposed methods is lower than that the conventional method. Also, our results show that the proposed convertor designed by technology 65nm, not only increases speed and decreases hardware size but also leads to a reduction in consumption power by approximately 90%.

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