Spectrum Sensor Hardware Implementation Based on Cyclostationary Feature Detector

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ABSTRACT:
Cognitive radios utilize spectrum sensors to provide information about the surrounding radio environment. This enables cognitive radios to communicate at the same frequency bands with existing (primary) radio systems, and thereby improve the utilization of spectral resources. Furthermore, the spectrum sensor must be able to guarantee that the cognitive radio devices do not interfere with the primary system transmissions. This paper describes a hardware implementation of a spectrum sensor based on cyclostationary feature detector, which has an improved detection performance achieved by decimation of the cyclic spectrum. Decimation also provides a simple way to control detection time and, therefore, allows trading the detection time to better probability of detection and vice versa. Implementation complexity in terms of power consumption and silicon area for a 65 nm CMOS process is evaluated. Measured detection performance is presented and detection of a 802.11g WLAN signal through air interface is demonstrated.

KEYWORDS: cognitive radio, CR, wireless, spectrum sensing, feature detector, cyclostationary, FPGA.

1. INTRODUCTION

As wireless communications systems evolve, demand for spectral resources is continuously growing. However, traditional frequency allocation policy has resulted in a situation where unallocated spectrum bands are running short, while measurements have shown that spectrum utilization in already allocated bands is usually low.

Cognitive radios (CR) [1][2] promise a solution for taking advantage of underutilized spectral resources and have been a popular research topic for several years. Cognitive radio's capability to recognize the surrounding radio environment and operate accordingly (i.e. change operation frequency, modulation etc.) permits operation among existing communication systems without interfering the primary users. This enables major increase in spectrum utilization.

To produce awareness of the surrounding radio spectrum, cognitive radio device needs to incorporate a spectrum sensing unit, which is able to sense spectral opportunities reliably and at very low signal-to-noise ratios (SNR). Furthermore, appearance of the primary user must be detected in reasonable time to minimize interference produced by the secondary network to the primary system.

Spectrum sensing can be implemented for example with energy detectors or feature detectors such as cyclostationary based detectors [3][4]. Energy detectors are very simple to implement, but their performance degrades when noise levels are unknown and they are also incapable to differentiate between signals from various systems [5]. Therefore, energy detectors are best suited for fast and coarse spectrum scanning. Feature detectors, in general, can operate reliably at very low SNR levels and can also differentiate certain signal types from others.

Much of the recent work is concentrated on IEEE802.22 [6]-[8], which is the first standard based on cognitive radio technology. It defines a radio interface for Wireless Regional Access Network (WRAN) that operates at the frequency bands currently mainly occupied by digital TV broadcast services. In IEEE802.22 networks, sensing task is somewhat simplified due to two facts. Firstly, primary signals that must be detected include only DTV broadcasts and Part 74 (wireless microphones etc.) transmissions and, thus, purpose-built sensing algorithms can be used. Secondly, locations of both base stations and customer equipment are fixed, which relaxes implementation constraints. Practical spectrums sensor implementations for DTV bands have been presented in [9].

A more general approach is taken in this work. The detection algorithm, presented in Section 2, is based on cyclostationarity that the received signal inherits for

example from modulation, cyclic prefixes or spreading codes. Since the parameters are system dependent, cyclostationarity can be used to identify the received signal. Detectors based on cyclostationarity have been presented in [10]-[12]. Effort is put especially on identifying OFDM-based (orthogonal frequency division multiplex) systems (e.g. WLAN, DVB-T, LTE), which is likely to be used in many future systems, but the concept is extendable to other signal types as well [13].

In general, detector performance is characterized by two metrics: probability of detection and false alarm rate. They are both equally important, since low probability of detection increases the amount of interference inflicted on the primary users, whereas high false alarm rate increases the amount of missed spectral opportunities in the secondary network. Other important parameters are the detection time resolution and bandwidth, and, of course, power consumption and area of the implementation.

This paper is organized as follows: Section 2 presents the cyclostationary feature detection algorithm and shows how decimation can be utilized to control the detection time, therefore resulting in fixed-length FFT implementation. Section 3 describes both the algorithm implementation and the hardware used to implement the spectrum sensor prototype platform. Section 4 then presents measured detector performance (probability of detection) and compares it to ideal performance from Matlab simulations. Moreover, over-the-air sensing is demonstrated with 802.11g WLAN signal. Finally, a conclusion is given in Section 5.

2. ALGORITHM DESCRIPTION

A process x(t) is second-order cyclostationary if its mean and autocorrelation are periodic in time [14]. Thus, for a cyclostationary process, the cyclic autocorrelation function (CAF) is nonzero for a set of cyclic frequencies $\alpha \neq 0$. Here, we concentrate on signals that exhibit conjugate cyclostationarity such as OFDM signals. The conjugate cyclic autocorrelation function at cyclic frequency α can be estimated as

$$\widehat{\mathrm{R}}_{\mathrm{x}}^{\alpha} = \frac{1}{N}\sum_{n=0}^{\mathrm{N}-1} \mathrm{x(n)x^{*}(n-\tau)e^{-\frac{j2\pi\alpha n}{N}}} = \mathrm{R}_{\mathrm{x}}^{\alpha} + \varepsilon(\alpha) \quad (1)$$

in which ε(α) is the estimation error. Here, τ is lag parameter in the autocorrelation. In practice, values of the CAF are seldom exactly zero and decision has to be made whether the value presents a zero or not.

If the cyclic autocorrelation does not exist, $R_x^{\propto} = 0$ and $\hat{R}_x^{\propto} = \varepsilon(\alpha)$, which is asymptotically normal zero mean complex random variable

$$\widehat{\mathrm{R}}_{\mathrm{x}}^{\alpha} = \varepsilon(\alpha) = X(\alpha) + jY(\alpha) \quad (2)$$

X(α) and Y(α) are normal distributed zero mean random variables. For vector of zero mean random variables, an estimate of the covariance matrix can be computed as

$$\hat{\Sigma}_{2c} = \begin{bmatrix} E[X^2] & E[XY] \\ E[XY] & E[Y^2] \end{bmatrix} \quad (3)$$

where elements of the matrix are

$$E[X^2] = \frac{1}{N}\sum_{k=0}^{\mathrm{N}-1} \Re\{\widehat{\mathrm{R}}_{\mathrm{x}}^{\alpha_k}\}^2 \quad (4)$$

$$E[Y^2] = \frac{1}{N}\sum_{k=0}^{\mathrm{N}-1} \Im\{\widehat{\mathrm{R}}_{\mathrm{x}}^{\alpha_k}\}^2 \quad (5)$$

$$E[XY] = \frac{1}{N}\sum_{k=0}^{\mathrm{N}-1} \Re\{\widehat{\mathrm{R}}_{\mathrm{x}}^{\alpha_k}\}\Im\{\widehat{\mathrm{R}}_{\mathrm{x}}^{\alpha_k}\} \quad (6)$$

The error introduced to expectation by cyclic frequency component $R_x^{\propto}$, if it exists, is not significant in critical cases (low SNR), and converges to zero with large N.

In order to find out if cyclic components exist in $\hat{R}_x^{\alpha}$, a hypothesis test is developed by following the guidelines presented in [10]. Hypotheses are

H_0: $\forall \alpha \in A \rightarrow \hat{R}_x^{\alpha} = \varepsilon(\alpha)$ (7)

H_1: $for\ some\ \alpha \in A \rightarrow \hat{R}_x^{\alpha} = \mathrm{R}_{\mathrm{x}}^{\alpha} + \varepsilon(\alpha)$, (8)

where set A contains all cyclic frequencies for a fixed value of τ, which are assumed to be known a priori. Under null hypothesis, test statistic

$$\mathrm{T} = \left(\widehat{\mathrm{R}}_{\mathrm{x}}^{\alpha}\right)\left(\hat{\Sigma}_{2c}\right)^{-1}\left(\widehat{\mathrm{R}}_{\mathrm{x}}^{\alpha}\right)^{\mathrm{T}} \quad (9)$$

Is χ_2^2-distributed and the following constant false alarm rate test for presence of cyclostationarity is derived:

$$F_{\chi_2^2}(\mathrm{T}) = 1 - \mathrm{p} \quad (10)$$

$F_{\chi_2^2}$ is the cumulative distribution function of χ_2^2-distribution and p is the false alarm rate. The test can be modified to include multiple lag values [10] and/or cyclic frequencies [11]. An alternative approach to estimate the covariance matrix is presented in [10].

In the derivation of the algorithm, samples of the process x(t) are assumed to be well separated in time and thus approximately independent. In practice, however, presence of a narrowband interferer or spectral shaping of the noise (channel filtering) violate this assumption and may affect the detector performance. Aforementioned phenomena exist at some level in all practical radio receivers and needs to be acknowledged in the design of the detector.

Often the information in the cyclic spectrum resides on low cyclic frequencies. Therefore, the high end of the cyclic spectrum is of no interest and the

Autocorrelation product can be resampled at lower frequency. This is illustrated in Fig. 1, where a cyclic spectrum of an OFDM signal is simulated without decimation. In Fig. 2 the simulation is repeated and decimation by 8 is applied.

Decimation increases the detection time by a factor corresponding the decimation ratio, and therefore improves the probability of detection. This is because a longer signal can be processed with a fixed-length FFT. Maximum decimation ratio depends on cyclic frequencies of the signal under detection, or can also be limited by detection time constraints either from the

cognitive radio system or from the duration of the transmission of the primary system signal.

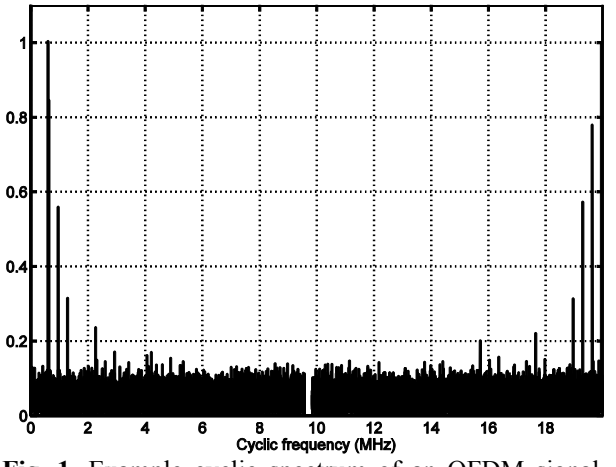

Fig. 1. Example cyclic spectrum of an OFDM signal sampled at 20MHz. Number of subcarriers is 52 and length of cyclic prefix is 12.

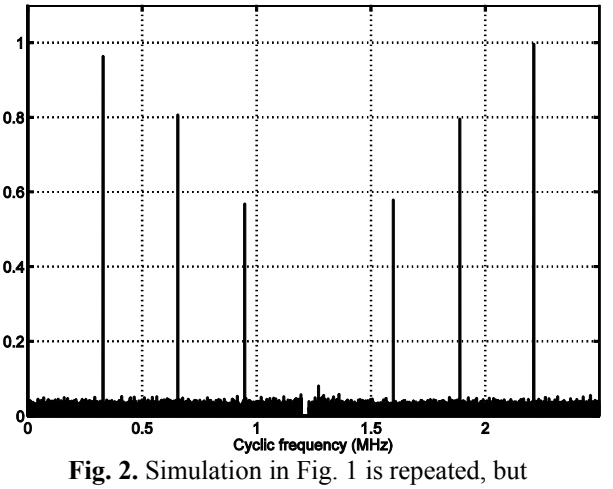

Fig. 2. Simulation in Fig. 1 is repeated, but autocorrelation signal is now decimated by factor of 8.

3. IMPLEMENTATION

The cyclostationary feature detection algorithm was implemented to calculate the test statistics (9), which can be then compared to the pre-calculated threshold (10) to make a decision if the primary signal is present or not. Multiple choices exist for calculating the multiplication with the exponential term followed by:

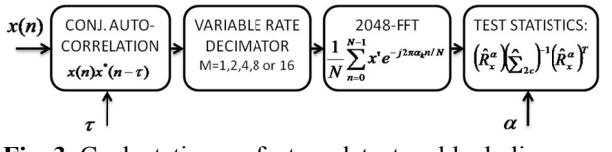

Fig. 3. Cyclostationary feature detectors block diagram.

The summation in (1). FFT was selected for the calculation, as it gives not only the cyclic frequency bin of interest but the whole cyclic spectrum for a fixed lag value. This provides insight to the operation of the algorithm and also enables implementation of tests based on multiple cyclic frequencies. In addition, the FFT can be reused for implementing spectrum estimation based energy detectors with small extra hardware. A somewhat simpler implementation could be, for example, to use a CORDIC [15] for a frequency shift followed by an integrator for the summation, which would have the downside of supporting a single cyclic frequency only.

The selected implementation is shown in Fig.3. First, complex input signal, sampled at 20 MHz, is multiplied with delayed version of itself. The autocorrelation requires a complex multiplier and a dual-port random access memory (RAM) to implement the lag, as shown in Fig. 4. Size of the memory is determined by expected maximum lag value and depends directly on the set of primary systems that one wants to detect. For example, delay of 64 baseband samples is enough for 802.11g WLAN signal, but it could be as high as 8192 samples for example in DVB-T systems.

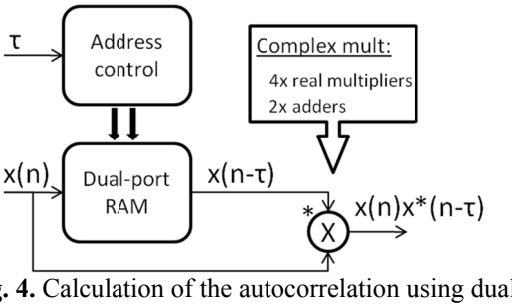

Fig. 4. Calculation of the autocorrelation using dual-port RAM and a complex multiplier.

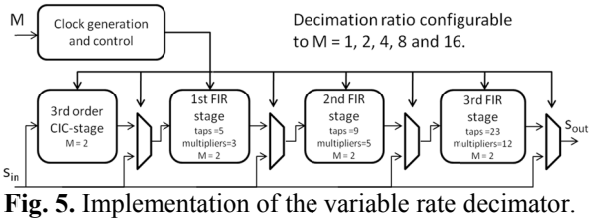

Fig. 5. Implementation of the variable rate decimator.

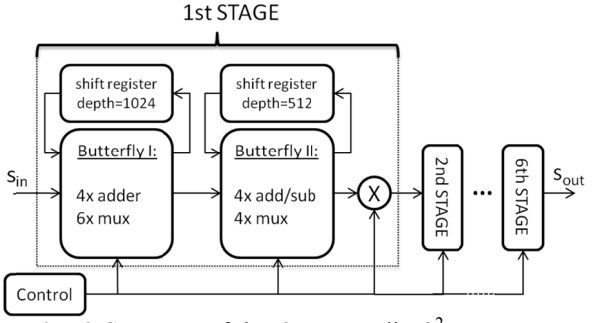

Fig. 6. Structure of the 6-stage radix-2^2 DIF FFT.

The autocorrelation product is then resampled using variable rate decimator that is presented in Fig. 5. The decimator consists of a CIC-stage [16] and three decimate-by-2 stages that were implemented using FIR filters. This combination supports decimation ratios M=1,2,4,8 and 16. The CIC-stage was included to allow future implementation of higher decimation ratios with simple modifications to the control logic and clocking circuitry.

Following the decimator is the FFT processor. 2048-point radix-2^2 DIF FFT algorithm [17] was selected because of its relatively low complexity, small area and power consumption. It is a pipelined architecture that is suitable for real-time high-speed applications (Fig. 6). Normally this type of FFT requires a reordering memory block, since the pipeline output samples appear in bit-wise reversed order. In this application reordering is not necessary, since the test statistics can be calculated from the unordered set of values as well.

Finally, the test statistics is calculated as presented in (9). First, elements of the covariance matrix (4)-(6) are calculated from the FFT output using three multiply-and-accumulate blocks. FFT output samples at the specified cyclic frequency, denoted by $r = \Re\left(\widehat{\mathrm{R}}_{\mathrm{x}}^{\alpha}\right)$ and $i = \Im\left(\widehat{\mathrm{R}}_{\mathrm{x}}^{\alpha}\right)$, are stored in temporary registers.

Calculating the matrix inversion, (9) can be rewritten as

$$\mathrm{T} = \frac{\mathrm{r}^2 E[Y^2] + \mathrm{i}^2 E[X^2] - 2riE[XY]}{E[X^2]E[Y^2] - E[XY]^2} \qquad (11)$$

which shows how the test statistics can be obtained with 7 multiplications, 3 additions/subtractions and one division.

The FFT dictates the detection time, i.e. the time interval over which test statistic is calculated. The detection time and can be expressed as

$$\mathrm{T_d} = \frac{M * N_{FFT}}{f_{s,in}} \qquad (12)$$

where $f_{s,in}$ is the input sampling frequency, M is the decimation ratio and N_{FFT} is the size of the FFT which is fixed to 2048. By adjusting the decimation ratio before the FFT, better detection performance is obtained via increased detection time. For example, T_d ranges from 102 µs (M=1) to 1.6 ms (M=16) when input is sampled at 20 MHz. In addition, using higher decimation ratio also decreases power consumption, since most of the logic is then sampled at lower clock frequency and power consumption of CMOS logic is approximately directly proportional to the sampling frequency.

A block diagram of the spectrum sensor hardware is presented in Fig. 7. It contains a commercial WLAN RF receiver and a 10-bit 80-MSPS A/D converter for signal reception. The core of the sensor is an FPGA circuit, which implements digital baseband block for channel filtering and DC cancellation, the presented detection algorithm, a central control unit, and a NIOSII processor for handling the communications with the outside world via USB. On the other end, a laptop PC running Matlab is used to implement a user interface. Fig. 8 shows a photo of the spectrum sensor hardware.

Complexity of the detector implementation was estimated by synthesizing the VHDL to a 65 nm CMOS process. The design was not optimized for an ASIC implementation in any manner; especially the memories in both autocorrelation and FFT were implemented with power and area consuming standard logic registers. Nevertheless, the worst-case power consumption estimate at 20 MHz operating frequency was 14.2 mW and silicon area approximately 1.0 mm^2. The figures show that the complexity is rather small compared to a wideband front-end. Moreover, since the memory blocks are the most power and area consuming parts in the design, the figures are expected to go down significantly when replaced with real memories.

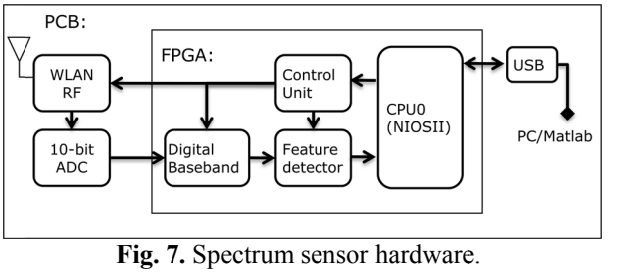

Fig. 7. Spectrum sensor hardware.

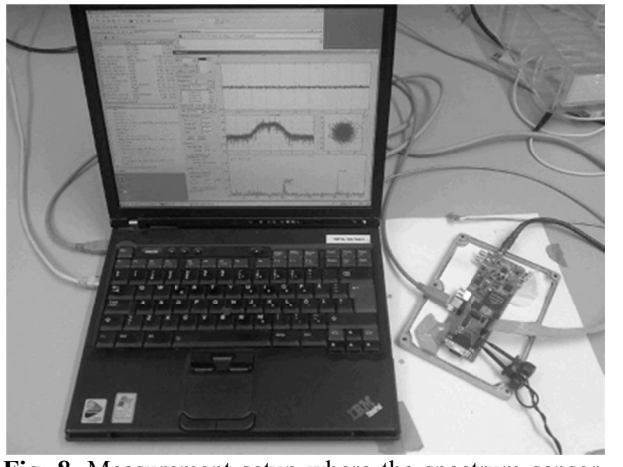

Fig. 8. Measurement setup where the spectrum sensor is connected to laptop via USB and user control interface is running in Matlab.

4. SIMULATION/MEASUREMENT RESULTS

Detector performance was first evaluated with a Matlab model of the detection algorithm. The model is consistent with the FFT-based approach, presented in Section 3, including the FFT and the decimation filters. The model is tested with a signal that utilizes OFDM modulation with 52 subcarriers (N_{FFT}), the length of

the cyclic prefix is 12 samples (N_{CP}) and subcarrier modulation employed is 16-QAM. Due to the cyclic prefix, autocorrelation of the OFDM symbol stream is periodic with delay $\tau = 52$ and the fundamental period is 64 samples (N_{FFT}+N_{CP}). Consequently, the signal has a cyclostationary feature at cyclic frequency $\alpha = f_s/64$.

Fig. 9 shows simulated probability of detection as a function of SNR for different decimation ratios (*M*). Probability of false alarm is set to 0.05 and noise is additive white Gaussian (AWGN). The simulation shows that increasing the decimation ratio by a factor of two, which doubles the length of the processed signal, yields better detection performance, as the same probability of detection is then achieved at approximately 1.5 dB lower SNR. Furthermore, the signal is detected reliably (95% probability of detection) 10 dB below the noise floor with maximum decimation ratio *M*=16.

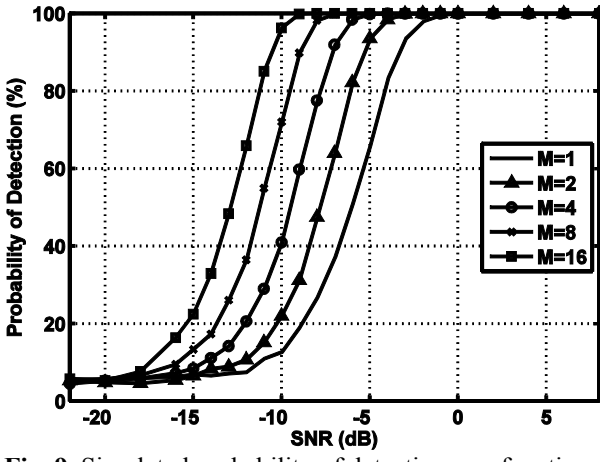

Fig. 9. Simulated probability of detection as a function of SNR for multiple decimation ratios (M).

Performance of the FPGA implementation was verified by measuring detection probability of the same OFDM signal that was used in the simulations. Anritsu MG3700a vector signal generator was used to modulate the baseband signal to WLAN channel 1 (2.412 GHz) and the signal was brought to test board's antenna connector. Fig. 10 presents measured probability of detection as a function of input power to the antenna connector. With the highest decimation ratio, reliable detection is obtained with input power as low as -106 dBm. This is approximately 5 dB below the thermal noise floor for 20 MHz bandwidth, which is

$$P_n = -174 + 10\log(20 * 10^6) \approx -101\ dBm. \quad (13)$$

Fig. 11 compares the measured and simulated detection performances (*M*=16) by mapping the zero SNR point to the thermal noise floor. Moreover, it should be noted that the simulation assumed a noiseless receiver whereas measured noise figure (NF) of the receiver is 4.7 dB. The difference between simulated and measured probability of detection matches well with the receiver NF. This also shows why NF as small as possible is desirable in the receiver since it is directly translated into a decrease in the sensitivity of the spectrum sensor.

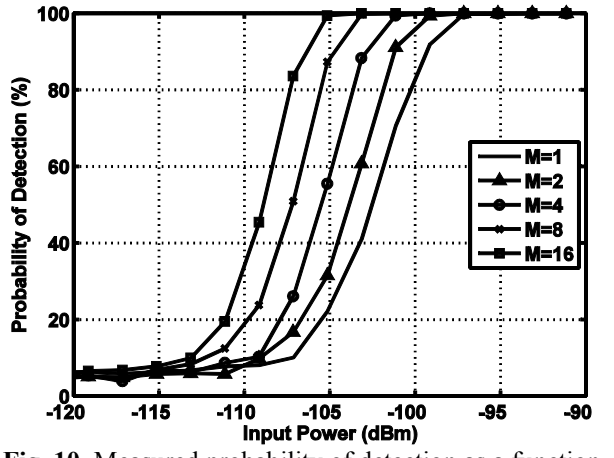

Fig. 10. Measured probability of detection as a function of input power to the RF receiver. Measurement uses the same OFDM signal that was simulated in Fig. 6.

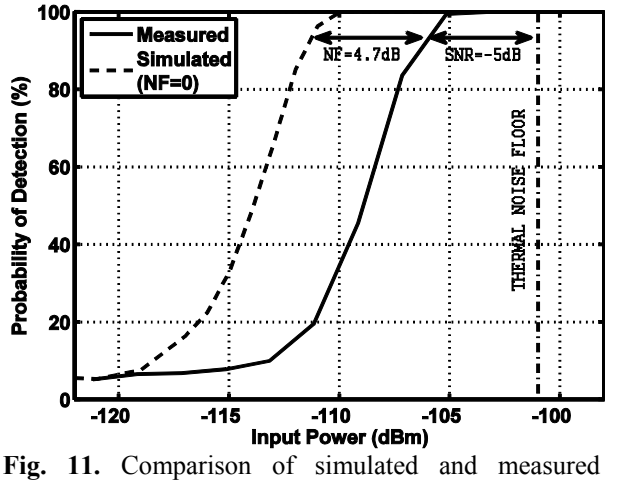

Fig. 11. Comparison of simulated and measured detection probabilities (*M*=16). The difference is 5 dB of which 4.7 dB comes from the receiver noise figure (NF) which is not included in the simulation.

Finally, detection of 802.11g WLAN signal from air was demonstrated. In this case, WLAN traffic was generated with a laptop, which was located in the same room with the detection equipment. 802.11g OFDM-signal has FFT/IFFT period (T_{FFT}) of 3.2 s, which corresponds to 64 samples at 20 MHz sampling frequency. Therefore, primary signal's cyclostationary feature is found by setting the lag parameter to 64. The signal exhibits cyclostationary with cycle frequency $\alpha = (T_{FFT} + T_{CP})^{-1}$ = 0.25 MHz, where T_{CP} = 0.8 μs is the length of the cyclic prefix. This can be observed

from the measured cyclic spectrum that is presented in Fig. 12. Detections in time are presented over 400 ms period in Fig. 13. Black lines correspond to time instances where WLAN signal was detected. In the measurement detection time resolution was set to 0.82 ms. In between the primary signal transmissions, spectral opportunities in the order of tens of milliseconds can be observed in this example.

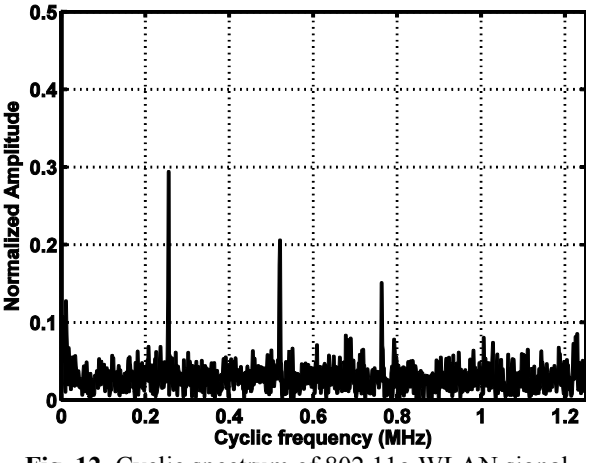

Fig. 12. Cyclic spectrum of 802.11g WLAN signal measured over-the-air.

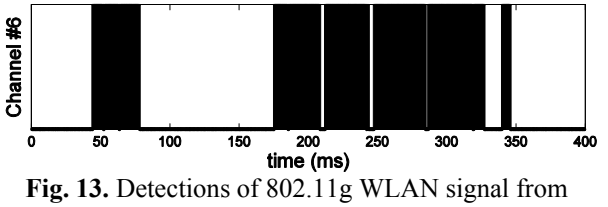

Fig. 13. Detections of 802.11g WLAN signal from channel 6 (2.437 GHz) over 400 ms period.

5. CONCLUSION

Implementation of a cyclostationary feature detector for spectrum sensing in cognitive radios was described. It was shown how decimation of the received signals autocorrelation product can be used to control the detection time in a fixed-size FFT implementation, thereby allowing flexible operation in an environment where multiple different primary systems might exist. Furthermore, feasibility of the design in respect of power consumption and silicon area was proved by synthesizing the design to a 65 nm CMOS process. Reference simulation results were provided and the measured detection performance of an ODFM signal was shown to match well with the simulations. The reference signal was detected with 95% probability when the received power was only -106 dBm (20 MHz bandwidth). Finally, detection of 802.11g WLAN signal was demonstrated through air interface.

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