Overview of low-voltage low-power design techniques and design of a low-voltage low-Power low-noise operational amplifier

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ABSTRACT:
In this paper an overview of circuit techniques dedicated to design low-power low-voltage is presented. These techniques (a) dynamic threshold voltage MOSFET (DTMOS) (b) bulk-driven and (c) current-driven bulk (CDB) are applied to design low-power low-voltage and low-noise CMOS operational amplifier (op amp) using sub-threshold region of MOSFET for bio-medical instrumentation operating with a 0.6 V supply. The operational amplifier is designed and simulated using TSMC 0.18µm CMOS technology. With DTMOS technique, the open loop gain is 60.51 dB, the unity gain-bandwidth (UGBW) is 12.08 kHz, phase margin is 52.3 degree and power consumption is 53.21 nW. With bulk-driven technique, the open loop gain is 49.04 dB, the unity gain-bandwidth is 3.32 kHz, phase margin is 71.96 degree and power consumption is 53.3 nW. With CDB technique, the open loop gain is 53.54 dB, the unity gain-bandwidth is 19 kHz, phase margin is 50 degree and power consumption is 55.79 nW. DTMOS technique provides high open loop gain, CDB technique provides high unity gain-bandwidth and bulk-driven technique provides better phase margin. Also DTMOS technique has less input-referred noise than the other methods.

KEYWORDS: Bulk-driven, Current-driven bulk, CDB, DTMOS, Low-power, Low-voltage, Low-noise, Operational amplifier, Op amp, Sub-threshold.

1. INTRODUCTION

In the past few years with the rapid growth of market for portable devices such as cell phones, portable computers and medical electronic implant devices, design of analog integrated circuits at low-power with high performance has become an extremely important issue.

Low-power op amp can be used as bio-potential amplifier. The basic purpose of a bio-potential amplifier is to amplify and filter the extremely weak bio-potential signals. The challenges of designing a bio-potential amplifier for bio-medical devices are high CMRR, low-noise for high signal quality and low-power dissipation. In bio-medical field low-power op amp require small bandwidth.

Reduction of threshold voltage is necessary for low-power low-voltage operation, so various techniques have been proposed for low-power low-voltage analog integrated circuits design. A MOSFET can be operated at a lower-voltage by forward biasing the source-bulk junction (bulk-driven technique). This approach has been used to design a low-power low-voltage CMOS operational amplifier, but with increasing forward body-bias, the leakage current increases significantly. The DTMOS technique in 1994 (Assaderaghi et al) is proposed to overcome the drawback in a forward-biased MOSFET [1]-[3]. This technique can be used in connection with the back-gate forward-bias technique in designing low-power low-voltage analog, digital and mixed signal CMOS integrated circuits. The current-driven bulk technique was first proposed in 2001 (T. Lehmann and M. Cassia). This technique is an efficient and robust method to achieve the maximum allowable forward biasing, without having large parasitic currents flowing in the well or in the substrate [4], [5].

Several papers have been focused on design of CMOS operational amplifier and operational transconductance amplifier (OTA) based on DTMOS, bulk-driven and CDB techniques. (a) DTMOS technique, in [6]-[9] the authors presented a novel class AB op amp for low-voltage (1 V) applications. In [10] the authors proposed an ultra-low-voltage ultra-low-power operational transconductance for biomedical applications. In [11] the authors presented a 0.8 V class-AB linear OTA for high-frequency applications. In [12] a novel input stage for low-voltage low-power and low-noise operational amplifier has been described. (b) bulk-driven technique, in [13] 0.5 V ultra-low-power OTA is presented. In [14] a novel

0.9 V OTA with dual bulk-driven input stage is introduced. In [15] 1 V low-power op amp is proposed. (c) CDB technique, in [4], [16] 1 V CMOS cascade amplifier is presented. In [17] a 1 volt rail-to-rail input range amplifier has been proposed. In [18] a gain-enhanced high-speed single-stage class-AB low-power op amp is presented.

The organization of this paper is as follows. In Section 2, the low-power low-voltage techniques are presented. In section 3, the sub-threshold operation is discussed. The structure of designed op amp is described in Section 4. The simulations results are provided in Section 5 and finally the conclusion is given.

2. LOW-POWER TECHNIQUES

An effective method for reducing power consumption is reduction the power supply voltage. A constraint to implementing digital and analog circuits at low-voltage is the threshold voltage. The minimum supply voltage is usually required to be at least equal to [5]:

$$V_{min} = V_{th,n} + |V_{th,p}| \quad (1)$$

Where $V_{th,n}$ and $V_{th,p}$ are the threshold voltage of the n-type and of the p-type transistors.

2.1. Dynamic Threshold voltage MOSFET (DTMOS)

DTMOS technique is the best idea for reduction threshold voltage. The DTMOS technique reduces the transistor off-state leakage current and also reduces the threshold voltage during on-state ($V_{BS} > 0$) according to below equation [19]:

$$V_{th} = V_{th0} + \lambda\left(\sqrt{|2\phi_F - V_{BS}|} - \sqrt{|2\phi_F|}\right) \quad (2)$$

Where V_{BS} is the source-bulk voltage, V_{th0} the threshold voltage for $V_{BS} = 0$, λ is body effect factor with an approximate value between 0.3 to 0.4 $\sqrt{V}$, and ϕ_F is Fermi potential with a typical value in the range of 0.3- 0.4 V [19].

In DTMOS technique, the bulk is tied to its own gate as shown in Fig. 1.

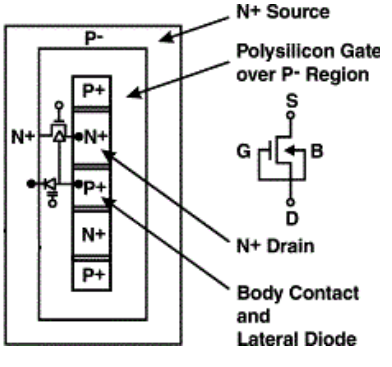


Fig. 1. Dynamic threshold MOSFET device [20].

This technique is limited to very low supply voltage. It cannot be applied to a circuit with a supply voltage over 0.8V. To apply this technique over a wide-voltage supply range, a reverse-biased MOS diode is inserted to suppress body leakage current. However, in a large complex chip with many transistors, this leakage current would become significant [21].

2.2. Bulk-driven

Bulk-driven technique was first proposed in 1987 (Guzinski et al) to overcome the threshold voltage [22]. Operating the MOS through the bulk-terminal allows the design of much low-supply voltage circuits. The operation of a bulk-driven MOSFET is similar to a JFET as shown in Fig. 2. The characteristics of the bulk-driven MOS can be summarized as, (1) large input common-mode range, (2) the small signal transconductance g_{mb} can even be larger than the MOSFET transconductance g_m and (3) high input impedance [5].

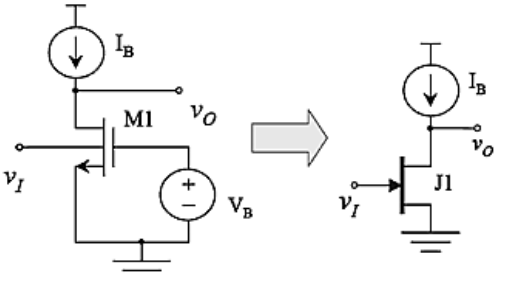


Fig. 2. Bulk-driven MOS transistor and its equivalent JFET.

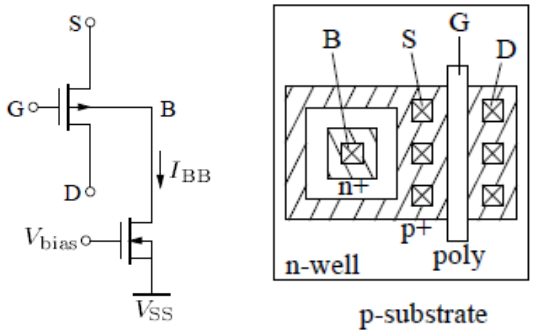
There are some drawbacks between bulk-driven devices compared to gate-driven devices. (1) Because of smaller transconductance, which results in higher input-referred noise. (2) The ground-connected gate terminals of the input pair will pick up any noise generated by the negative power supply. Therefore, the power supply rejection has poor performance. (3) Because of smaller control capacitance of the depletion layer, larger parasitic capacitance to the substrate, which results in lower f_T [23].

$$f_{T,Bulk-driven} = \frac{g_{mb}}{2\pi(C_{SB} + C_{DB} + C_{B-sub})} \quad (3)$$

$$f_{T,Gate-driven} = \frac{g_{mb}}{2\pi C_{GS}} \quad (4)$$

2.3. Current-Driven Bulk (CDB)

Current driven-bulk technique that shown in Fig. 3 can be used to achieve low- power and low-voltage design. CDB as a technique to reduce the threshold voltage of MOS transistor in standard CMOS technology. This technique consists of a MOS with the bulk terminal connected to a current source.



(a) (b)

Fig. 3. (a) PMOS current-driven bulk, (b) Layout [4].

Injecting a current into the bulk in NMOS would change the acceptor concentration (N_A), which in turn, causes a decrease in the threshold voltage of NMOS. Same understanding is valid for PMOS and donor concentration by extracting an electron from bulk [24]. The relationship between threshold voltage and acceptor concentration in NMOS can be expressed using the following equations:

$$Q_{B0} = \sqrt{2q.N_A.\varepsilon_{si}|-2\phi_f|} \quad (5)$$

$$V_{th0} = \phi_{ms} - 2\phi_f - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_i}{C_{ox}} \quad (6)$$

Where Q_{B0} is the negative charge under the gate, q is the electron charge, ε_{si} is the permittivity of the silicon, ϕ_{ms} is the work function difference between the gate material and substrate, C_{ox} is the gate-oxide capacitance, Q_{ox} is the equivalent positive oxide charge and Q_i is the total interface charge.

The CDB technique adds a set of unwanted effects which might limit the applicability of this technique, (1) lowering of output impedance, (2) increasing impact of parasitic capacitances, (3) unknown parasitic bipolar gain and (4) increasing transistor noise [5].

3. SUB-THRESHOLD OPERATION

Operation of the MOS device in sub-threshold region is very important when low power circuits are desired. When the V_{GS} in the MOS transistor is less than the threshold voltage (V_{th}), the MOSFET works in sub-threshold region. The drain current I_D of a MOS transistor in sub-threshold region is based on the channel diffusion current and can be given by (7), when referred to source voltage [10].

$$I_D = I_S\left(\frac{W}{L}\right)\exp\left(q\frac{V_{GS}-V_{th}}{nKT}\right)\left[1-\exp\left(-q\frac{V_{DS}}{KT}\right)\right] \quad (7)$$

Where I_S is the characteristic current, T is the absolute temperature, n is the slope factor, K is the Boltzmann constant and q is the charge of the electron or hole.

If $V_{DS} \geq 3KT/q$ then the transistor will be saturated in sub-threshold region. The transconductance g_m can be found as presented in (8), which is a function of current Ids and factor nKT/q [10].

$$g_m = q\frac{I_D}{nKT} \quad (8)$$

There is linear relationship between transconductance and current. Also transconductance is independent of device geometry. But in strong inversion relationship between transconductance and current is square law and also function of device geometry.

4. LOW-POWER LOW-VOLTAGE AND LOW-NOISE OPERATIONAL AMOLIFIER

In this paper, low-power low-voltage techniques have been applied on the low-noise op amp which proposed in [25]. The schematic of this op amp that shown in Fig. 4(a) is a modified version of a standard folded-cascode topology while working at sub-threshold region. Fig. 4(b) to 4(d) shows one typical application of a PMOS DTMOS, PMOS bulk-driven and PMOS current-driven bulk as in a differential pair.

The op amp in Fig. 4(a) is biased such that the currents of the transistors in the folded branch M7-M12 are only a small fraction of the current in the input differential pair transistors M1 and M2. Bias currents of M5 and M6 are provided through the use of the bias circuit formed by Mb2, Mc2 and Mc3. The current sources Mbl, Mb2 are cascoded to improve their output impedances and thereby ensure accurate current scaling. The source-degenerated current mirrors formed by Mc3, M5 and M6 and resistors R1 and R2 set the currents in M5 and M6 such that the currents in M7 and M8 are a small fraction of the currents in M1 and M2. The benefits of using source-degenerated current sources are, (1) the noise from resistors is mainly thermal noise while NMOS current sources contribute a large amount of *1/f* noise unless they are made with very large area and (2) the noise contributions from the source-degenerated current sources are mainly from the resistors and can be made much smaller than the noise contributions from MOS transistors operating at the same current level. The input-differential pair is made with large-area PMOS transistors, which have lower noise than similarly-sized NMOS transistors in most CMOS processes

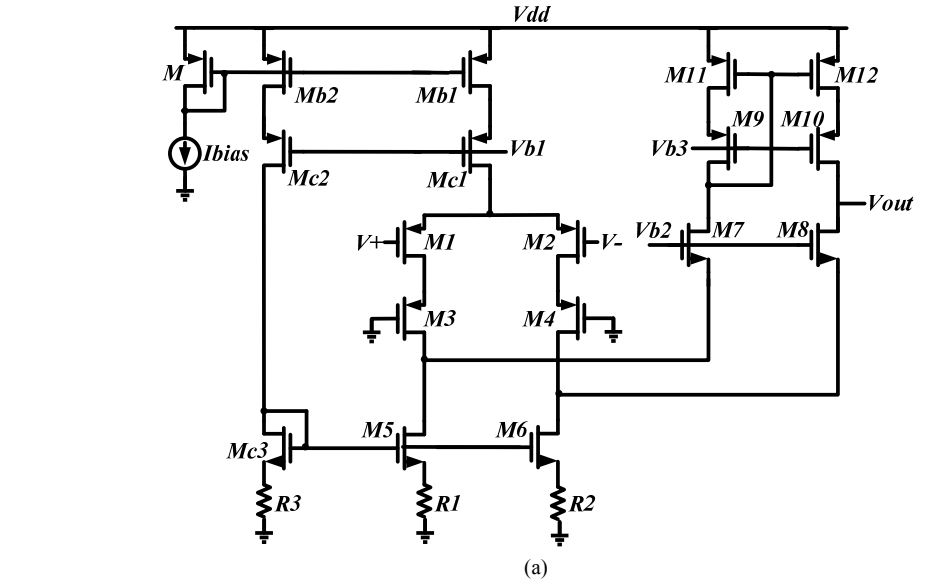
To have low input-referred noise, the transconductance G_m (near g_{m1}, the g_m of M1) of the op amp needs to be maximal for a given current level [25], [26]. Therefore, M1 and M2 need to have large *W/L* ration. The G_m is calculated by:

$$G_m = g_{m1}\cdot\left(\frac{G_{s7}}{G_{s7}+G_{ds}}\right)\left(\frac{G_{s3}r_{o1}}{1+G_{s3}r_{o1}}\right) \quad (9)$$

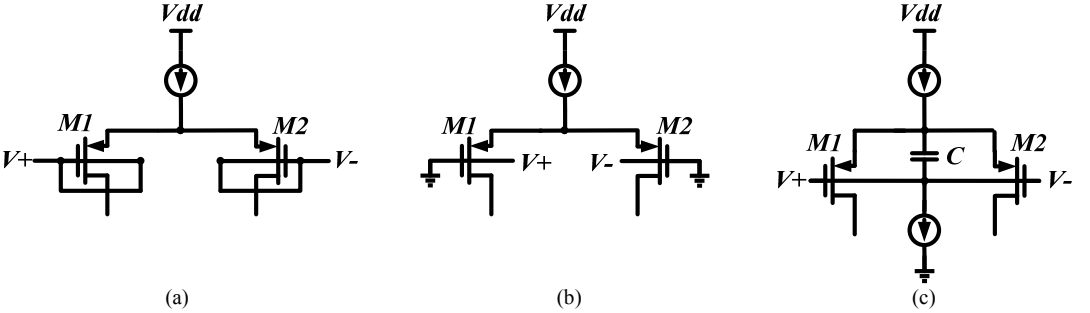
Where,

$$G_{s7} = \frac{g_{s7}+1/r_{o7}}{1+\frac{(1/g_{m11})}{r_{o7}}} \quad (10)$$

$$G_{ds} = \frac{1}{r_{os}} \cdot \frac{1}{1 + R_1 / r_{os} + g_{mb} R_1} \quad (11)$$



(a)



(a) (b) (c)

Fig. 4. (a) Schematic of the op amp circuit, Differential pair: (b) DTMOS PMOS (c) Bulk-driven PMOS (d) CDB PMOS.

$$G_{gs} = \frac{g_{sn} + 1/r_{ub}}{1 + 1/(r_{os}(C_{gs} \mid C_{ds}))} \quad (12)$$

Where g_{si} and r_{oi} are the incremental source admittance of M_i with its drain at incremental ground, and the output resistance of M_i, respectively.

The input-referred noise of the op amp is given by:

$$\overline{V_n^2} = \frac{1}{g_{m1}^2}\left(\frac{4KTg_{m1}}{\kappa} + \frac{8KT}{R_1} + \frac{16}{3}KTg_{m11}\right) \quad (13)$$

Where κ (kappa) is the gate coupling coefficient which represents the coupling of the gate to the surface potential [27]:

$$\kappa = \frac{C_{ox}}{C_{ox} + C_{dep}} \quad (14)$$

Where C_{dep} is the depletion capacitance. In modern CMOS processes, kappa ranges between 0.6 and 0.8.

5. SIMULATION RESULTS

The described op amp is designed in sub-threshold region using TSMC 0.18µm CMOS technology with 0.6 V power supply and under 10pF load. The size of each transistor in the op amp is shown in Table 1.

Table 1. Size of transistors.

Transistor	W/L (µm/µm)
M1-M2	1200/2.8
M3-M4	400/2.8
M5-M6	30.4/4.5
M7-M8	9.8/7.3
M9-M10	3.5/2.2
M11-M12	4.5/2.1
Mb1, Mb2	11/2.8, 14/4.6
Mc1, Mc2, Mc3	11/2.8, 14/4.6, 30.4/4.5
M	14/4.6

Typical Op amp performance such as power consumption, open loop gain, phase margin, unity-gain bandwidth, input-referred noise, power supply rejection

ratio (PSRR) and common mode signal rejection ratio (CMRR), etc. have been simulated at TT corner for all techniques. Simulation results for AC analysis for gain and phase plot vs. frequency is shown in Fig. 5. According to this figure, with DTMOS technique, the open loop gain is 60.51 dB, the unity gain-bandwidth is 12.08 kHz and phase margin is 52.3 degree, with bulk-driven technique, the open loop gain is 49.04 dB, the unity gain-bandwidth is 3.32 kHz and phase margin is 71.96 degree and with CDB technique, the open loop gain is 53.54 dB, the unitygain-bandwidth is 19 kHz and phase margin is 50 degree.

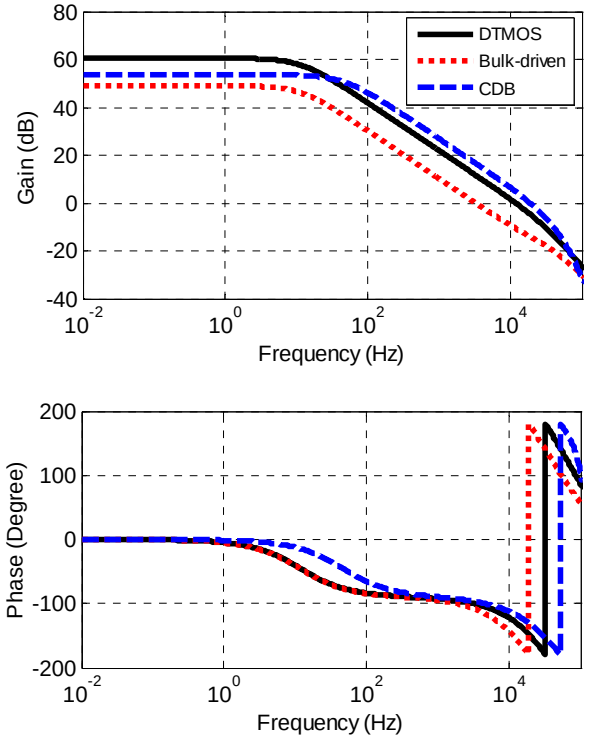


Fig. 5. Simulated open loop gain and phase margin.

The CMRR of the op amp which shown in Fig. 6 for DTMOS, bulk-driven and CDB techniques is 114.6 dB, 118.6 dB and 103.8 dB respectively. The bulk-driven technique has a better CMRR than other techniques.

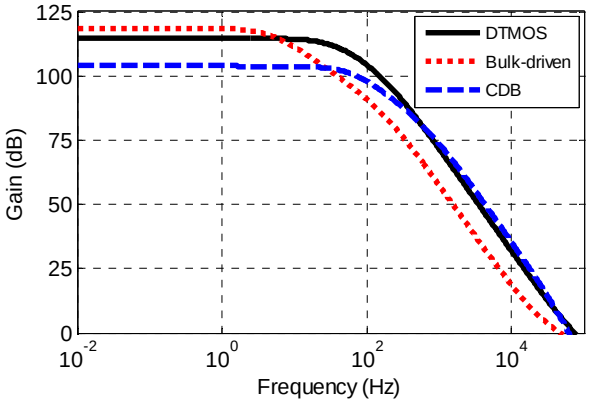


Fig. 6. Simulated CMRR.

The PSRR of the op amp which shown in Fig. 7 for DTMOS, bulk-driven and CDB techniques is 78.37 dB, 67.03 dB and 70.85 dB respectively. The DTMOS technique showed a better PSRR than other techniques.

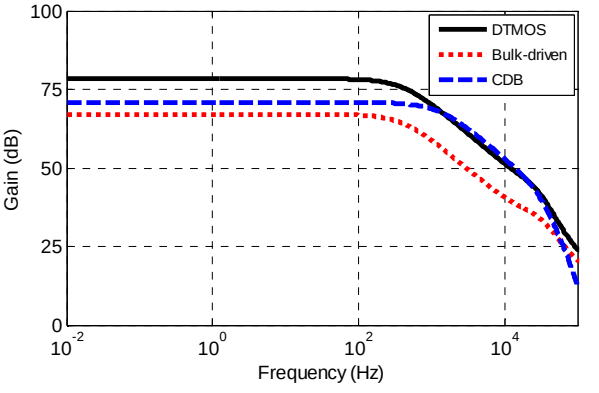


Fig. 7. Simulated PSRR.

The simulated input-referred voltage noise performance of the circuit is shown in Fig. 8. With DTMOS technique the input-referred noise is 40.58 pV/√Hz at 1 Hz and 0.177 pV/√Hz at 100 Hz, with bulk-driven technique the input-referred noise is 600.6 pV/√Hz at 1 Hz and 2.57 pV/√Hz at 100 Hz and with CDB technique the input-referred noise is 70.8 pV/√Hz at 1 Hz and 0.32 pV/√Hz at 100 Hz.

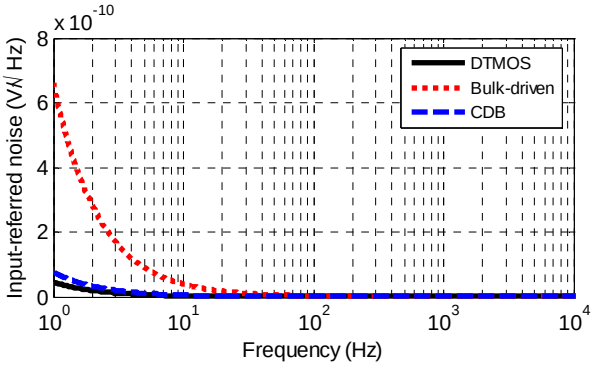


Fig. 8. Simulated input-referred noise.

Table 2 shows a comparison with other low-voltage low-power and low-noise operational amplifiers. To evaluate this work a figure of merit (FoM) is defined as [10]:

$$FoM = \frac{Gain * UGBW}{Power\ supply * Power\ consumption} \quad (15)$$

6. CONCLUSION

The design of an ultra-low-power ultra-low-voltage and ultra-low-noise, high performance operational amplifier in a 0.18 µm CMOS process using low-power

low-voltage techniques at sub-threshold region with 0.6 V power supply is reported in this paper. The simulation results show with DTMOS technique open loop gain is 60.51 dB and unity-gain bandwidth is 12.08 kHz, with bulk-driven technique, the open loop gain is 49.04 dB and the unity gain-bandwidth is 3.32 kHz and with CDB technique, the open loop gain is 53.54 dB and the unity gain-bandwidth is 19 kHz. Power consumption in three techniques approximately is 54 nW. The low gain and unity-gain bandwidth disadvantages of the bulk-driven technique are circumvented by employing DTMOS technique or CDB techniques. However bulk-driven technique has a better phase margin and CMRR than other techniques.

The DTMOS technique is useful for biomedical application, because this technique has less input-referred noise. As a conclusion, we can say that DTMOS and CDB techniques are very suitable to design low-power low-voltage and low-noise circuits, especially for medical applications.

Table 2. Comparison between operational amplifiers.

	Process (µm)	V_{dd} (V)	Power (nW)	Gain (dB)	Phase margin (Degree)	UGBW (kHz)	CMRR (dB)	PSRR (dB)	Input-referred noise $\left(\frac{pV}{\sqrt{Hz}}\right)$	C_{Load} (pF)	FOM
DTMOS	0.18	0.6	53.21	60.51	52.3	12.08	114.6	78.37	40.58 @ 1 Hz	10	22.9
Bulk-driven	0.18	0.6	53.3	49.04	71.96	3.32	118.6	67.03	600.6 @ 1 Hz	10	5.1
CDB	0.18	0.6	55.79	53.54	50	19	103.8	70.85	70.8 @ 1 Hz	10	30.39
[10]:DTMOS	0.18	0.4	386	91	66	111.4	106	N/A	500 @ 100mHz	15	65.66
[10]: Bulk-driven	0.18	0.4	386	78	N/A	16.6	93	N/A	N/A	15	8.39
[13]: Bulk-driven	0.18	0.5	1020	88.5	66.3	83.88	133.85	N/A	N/A	15	14.47
[17]: CDB	0.18	1	187000	71	78	8000	100	81	42000 @ 1 kHz		3.04
[18]: CDB	0.18	1.8	450000	83.7	87	69000	N/A	N/A	N/A	2	7.13

- FOM ($\frac{dB \cdot kHz}{V \cdot nW}$)

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