Implementation of RADAR Quadrature Channel Receiver in FPGA

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ABSTRACT:
In this paper we have presented the implementation of radar digital quadrature channel receivers in FPGA. Utilizing direct digitalization due to avoid improbable matching in producing in-phase (I) and quadrature (Q) signals, is greatly respecting in every modern system but this merit needs some considerations which are highlighted in the current paper. Two factors resource and maximum frequency for hardware implementation of proposed algorithm utilizing Virtex-5 ML506 are evaluated and compared with the customary algorithm of analog and digital receivers which generally utilize two mixers, lowpass filters and analog to digital converters for down converting signal from intermediate frequency to baseband. Also in this paper some simulations for different examples are illustrated.

KEYWORDS: Radar, Digital quadrature channel receiver, FPGA, IF sampling*;*

1. INTRODUCTION

Existence of two mixers even with unique clock reference usually cause to imbalance and matching problems which face I and Q demodulators with such difficulties that encourage radar engineers for digitalizing whole radar system. With the intention of avoiding aliasing Shannon theory states that the sampling frequency must be at least twice greater than signal bandwidth. In the case of baseband signals, sampling frequency need not to be less than half of the maximum frequency (Nyquist theory) [1]. But a signal of 5MHz bandwidth at intermediate frequency (IF) of 75MHz needs to be sampled at 160MHz according to Nyquist criteria. While it is problematic either to design or to find a high dynamic range ADC with high speed of acquisition simultaneously, it is considerable to sample the above signal with 10MHz frequency of sampling.

A traditional way for this subject was to mix the IF signal to the form of two parallel baseband channels with components of in-phase (I) and quadrature (Q), and sampling them with a lower rate. Phase errors of several degrees due to imperfect matching limit the achievable performance from signal processors such as moving target indicators, coherent integrators, Doppler filters, antenna array processors, and coherent sidelobe cancellers [2]. Undersampling or IF sampling is the other introduced method which is pondered nowadays due to its appreciated profits in designing digital receivers [3]. The desire toward digitalizing whole system between radar engineers is increasing nowadays with developing of technology such that it is imaginable to consider next generation radars with combination of radar antenna and signal processor unit [2]. But memory and speed limitations in implementation force designers to utilize fast and accurate algorithms as much as achievable. Therefore in this paper we have presented the implementation of fast or direct IF sampling method. The presented method is compared with the customary method in this paper.

This paper follows with description of digitally quadrature channel receiver in the following section where two considered method of digitally IF samplings are presented. Important considerations of fast under sampling are theme of third part of this paper. In the next section simulation and practical implementations are depicted. Finally conclusion represents main focus of this paper.

2. QUADRATURE CHANNEL RECEIVER

With the intention of avoiding customary errors of analog demodulators (amplitude error, phase error and

DC offset), utilizing digital quadrature detectors have been proposed in which baseband signals are created digitally according to "Fig. 1" block diagram.
For digital demodulation and producing I and Q signals, there are two regular methods which have described below.

2.1. First Method

In this method an ADC for digitalization of input IF signal is used. The mentioned demodulator utilize two digitally mixers and all relations are similar to analog customary quadrature detectors.
Consider IF signal with following equation in which $t = n\,T_s$,

$$V_{IF} = A_s\,sin(\omega t + \theta) = \frac{A_s}{2j}(e^{j(\omega n\,T_s+\theta)} - e^{-j(\omega n\,T_s+\theta)}) \quad (1)$$

We would have

$$V_{REF} = A_R[\sin(\omega_0 n\,T_s) + j\cos(\omega_0 n\,T_s)] = j\,A_R e^{-j\omega_0 n\,T_s} \quad (2)$$

And so

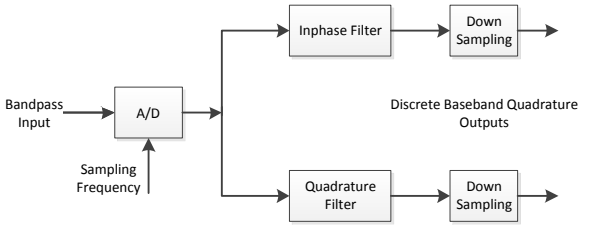

Fig. 1. Digital quadrature detectors

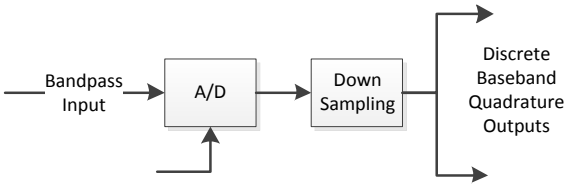

Fig. 2. Block diagram of IF sampling according to second method

$$V_{IF}V_{REF} = \frac{A_s}{2}(e^{j(\omega n\,T_s+\theta)} - e^{-j(\omega n\,T_s+\theta)})\,A_R e^{-j\omega_0 n\,T_s} \quad (3)$$

Result in

$$V_{IF}V_{REF} = \frac{A_s A_R}{2}e^{j[(\omega-\omega_0)n\,T_s+\theta]} - \frac{A_s A_R}{2}e^{-j[(\omega+\omega_0)n\,T_s+\theta]} \quad (4)$$

That shows resulted signal will have frequencies of (ω-ω_0) and (ω+ω_0). In order to omit upper frequency signal, need to utilize lowpass filters,

$$V_{Filt} = \frac{A_s A_R}{2}e^{j[(\omega-\omega_0)n\,T_s+\theta]} \quad (5)$$

And by utilizing Euler equality for the above equation,

$$V_{Filt} = \frac{A_s A_R}{2}\cos[(\omega-\omega_0)n\,T_s+\theta] + j\frac{A_s A_R}{2}\sin[(\omega-\omega_0)n\,T_s+\theta] \quad (6)$$

Therefore we can obtain I and Q signals as follow,

$$V_I = \frac{A_s A_R}{2}cos[(\omega-\omega_0)n\,T_s+\theta] \quad (7)$$

$$V_Q = \frac{A_s A_R}{2}\sin[(\omega-\omega_0)n\,T_s+\theta] \quad (8)$$

Or in the other form,

$$V_{Filt} = V_I + jV_Q \quad (9)$$

There is down sampling block after each filter in order to decrease number of sample in chip (simple pulse width).
The merit of the cited process to the other is its resistance to frequency varying. Complicated calculations are its demerit.

2.2. Second Method

The idea which is considered here is using undersampling and a replica of baseband signal without remixing of it [4]. Sampling block diagram of IF signal through the second method is demonstrated in "Fig. 2".
Consider that reflected bandpass signal is modeled as follows [5]:

$$V_{IF}(t) = A(t)\,sin(\omega t + \theta(t)) = A(t)\,cos(\omega t + \varphi(t)) \quad (10)$$

In which,

$$\varphi(t) = \theta(t) - \pi/2 \quad (11)$$

Intermediate frequency signal has the bandwidth of B here, which $B = f_H - f_L$. In order to evade aliasing for sampling frequencies (f_s) of smaller than $2f_H$we must have,

$$2B \le f_s \le f_L/l \quad (12)$$

In which l is a positive integer number? With t=n T_s=n⁄f_s we can write,

$$V(n) = A(n)\,cos(2\pi f_c\frac{n}{f_s} + \varphi(n)) \quad (13)$$

$$V(n) = A(n)\,cos(2\pi n(l+0.25) + \varphi(n)) \quad (14)$$

$$V(n) = A(n)\,cos(\frac{n\pi}{2} + \varphi(n)) \quad (15)$$

$$V(n) = V_I(n)\cos\left(\frac{n\pi}{2}\right) - V_Q(n)\sin(\frac{n\pi}{2}) \quad (16)$$

When n=0,1,2,3,…, equation (16) can be expressed as,

$$V(n) = \begin{cases}(-1)^{n/2}V_I(n), & n = even\\ (-1)^{(n+1)/2}V_Q(n), & n = odd\end{cases} \quad (17)$$

Equation (17) depicts that with choosing suitable values for n signals of I and Q can be directly computed through the following equations,

$$V_I(n) = [V(0), 0, -V(2), 0, V(4), 0, -V(6), 0, \dots] \quad (18)$$

$$V_Q(n) = [0, -V(1), 0, V(3), 0, -V(5), 0, V(7), 0, \dots] \quad (19)$$

It means that the need for utilizing mixers or filters have been brushed in the direct method. This will simplify the implementation. Pursuing the above relations lead to the following equation [6]:

$$f_{IF} = kf_s \pm \frac{f_s}{4} \quad (20)$$

In which k is an integer and is greater than one. Moreover f_s is the sampling frequency and f_ IF is the intermediate frequency in the above equation. This equation can also be written with the following declaration:

$$f_s = \frac{f_{IF}}{k \pm 1/4} \quad (21)$$

Obviously some considerations for utilizing the second method are essential to avoid aliasing. Even though choosing smaller intermediate frequency is desirable for IF sampling, it is not recommended for front-end designing and vice versa. The other condition which must be always considered is the Shannon criterion which states that the least sampling frequency must be greater than twice of baseband signal bandwidth.

3. IMPORTANT CONSIDERATIONS FOR FAST IF SAMPLING

In order to achieve a proper IF sampling some criterions and conditions are essential to be considered [7].

1- Implementing IF sampling can be done using ADCs which are created for this propose. In the other words, conventional ADCs with usage of sampling baseband signals are not appropriate for digital quadrature detectors.

2- Analog to digital module bandwidth must be greater than the maximum intermediate frequency of signal.

3- High quality for sample and hold block in ADC is essential.

4- In order to decrease undesired signals effects, utilizing a filter with equally bandwidth intermediate frequency signal is necessary.

5- Small phase noise and jitter in analog to digital converter is critical.

6- DC offset of signal can affect the IF sampling performance.

Although digitally quadrature detectors are highly demanded by radar engineers, small attention to the mentioned consideration may abolish its advantages. In addition IF sampling is desired when carrier information of a signal is not important and the merit is in the bandwidth.

4. SIMULATION AND IMPLEMENTATION

The surveyed and presented algorithm of IF sampling, have been implemented in FPGA Virtex-5 ML506 board. A field programmable gate array (FPGA) is a general-purpose integrated circuit that is "programmed" by the designer rather than the device manufacturer. Unlike application specific integrated circuit (ASIC), which can perform a similar function in an electronic system, an FPGA can be reprogrammed, even after it has been deployed into a system.

An FPGA is programmed by downloading a configuration program called a bitstream into static on-chip random-access memory. Much like the object code for a microprocessor, this bitstream is the product of compilation tools that translate the high-level abstractions produced by a designer into something equivalent but low-level and executable. Xilinx System Generator pioneered the idea of compiling an FPGA program from a high-level Simulink model.

Virtex®-5 ML506 FPGA editions is a feature-rich DSP general purpose evaluation and development platform. Developed to provide an easy-to-use high-performance programming solution, Xilinx offers a full range of configuration memories optimized for use with Virtex® and Spartan® FPGAs. A variety of on-board memories and industry standard connectivity interfaces add to the ML506's ability to serve as a versatile development platform for embedded applications. Therefore ML506 Development Kit is prepared a suitable structure using XC5VSX50T processor for digital signal processing applications based on FPGA [8].

In order to implementation in the mentioned hardware we have used the system generator which is a tool of designing, introduced by Xilinx Company. System Generator is a system-level modeling tool that facilitates FPGA hardware design. It extends Simulink in many ways to provide a modeling environment that is well suited to hardware design. The tool provides high-level abstractions that are automatically compiled into an FPGA at the push of a button. The tool also provides access to underlying FPGA resources through low-level abstractions, allowing the construction of highly efficient FPGA designs[9]. Therefore the system generator toolbox helps designer to provide some simulations in Matlab environment for implementation. After confirmation at simulation environment and approving the results, the system generator blockset produces HDL code which can be synthesized and implemented in FPGA.

Standard method of implementation of quadrature detector which proposes utilizing of two mixers in order has been illustrated at "Fig. 3". According to "Fig. 3", for sine and cosine producing of the 75MHz reference signal, we have used DDS core. The outputs of this core at input signal are sampled with rate of 100MS/s. The lowpass filter and decimation of 8 are applied at this block diagram. Respect to the simulation a sinusoidal input at 76MHz practically involved to the board which its data at workspace of Matlab is illustrated at "Fig. 4".

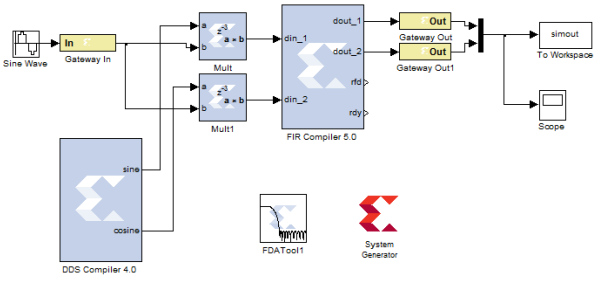

Fig. 3. Implementation of the first method using system generator

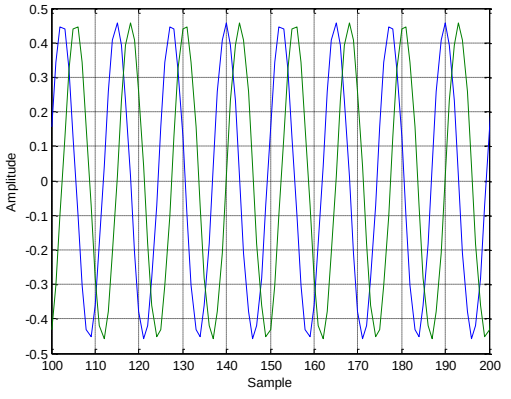

Fig. 4. Workspace output of the first method at Matlab

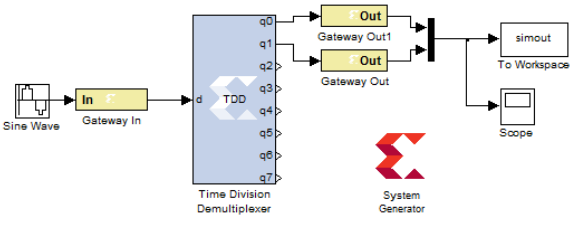

Fig. 5. Implementation of the second method using system generator

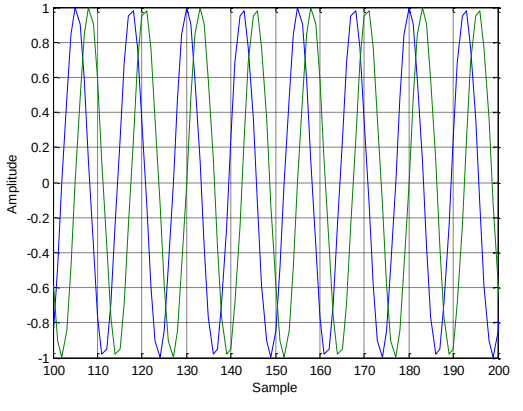

Fig. 6. Workspace output of second first method at Matlab

"Fig. 4" shows I and Q extracted signal with frequency of 1MHz. This method has the following advantages [4]:

- The least sampling frequency for each channel of I and Q could be achieved in this method and so that the slowest possible analog to digital converters can be utilized.
- Design and implementation of analog antialiasing lowpass filters, generally are easier to build, than there analog bandpass equivalents.

However it is very difficult to achieve phase and amplitude balance in both in-phase and quadrature signals with analog quadrature mixers.

The second method which have discussed before just needs to a decimator when we follow the discussed instructions. Time division demultiplexer blockset of "Fig. 5" converts directly IF signal to baseband of I and Q signals.

The extracted I and Q signals of "Fig. 6" illustrates same result with the first method. A comparison between these two methods respect to implementation has done in "Table 1".

Table 1. Comparison of occupied number of slices and maximum frequency of XC5VSX50T

	Maximum Frequency	Number of Slices
First Method	228MHz	744
Second Method	493MHz	61

As "Table 1"depicts maximum frequency of the second method is greater than two times of the first method. Also this method uses less number of slices which is important at real-time applications.

5. CONCLUSION

Nowadays trends in interest of sampling at higher frequencies between radar engineers are uprising. Radar designers hope to sample reflected signal at radio frequencies with curiosity but differences of analog and digital signals cause to different considerations in signal sampling which are illustrated in the current paper. Two digitally represented method of designing quadrature detectors have compared with each other in this paper and the result illustrated that the second method with some considerations can be easily implemented in digital area particularly at real-time applications.

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