Hybrid Frequency Compensation to Improve Unity-Gain Bandwidth of Low-Voltage Low-Power CMOS Operational Amplifiers

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ABSTRACT:
In this paper a new hybrid frequency compensation (HFC) technique consists of indirect compensation and compensation using unbalanced differential pairs for low-voltage low-power CMOS operational amplifiers (op amp) is proposed. This technique significantly improves frequency response of the op amp and avoids instability when a large capacitive load at the output of the op amp must be handled. Also, Dynamic threshold voltage MOSFET (DTMOS) and sub-threshold region are utilized in the design to effectively use the low supply voltage and reduce power consumption. To evaluate the proposed technique, the two stage operational amplifier is designed and simulated in a TSMC 0.18 μm CMOS process technology. The op amp operate at 0.6 V power supply with 138.3 nW power consumption. The proposed HFC technique uses a total compensation capacitance of 3.5 pF and is robust in stability under the variation of the load capacitance between 0 pF and 100 pF. When driving a 15 pF load, the proposed HFC amplifier reduces the total capacitor size 35% and improves the unity-gain bandwidth 481% compared to the conventional Miller compensation.

KEYWORDS: Op amp, Low-voltage low-power, Hybrid frequency compensation, Indirect compensation, Unbalanced differential pair.

1. INTRODUCTION

CMOS operational amplifiers have become of the most important building blocks in analog integrated circuits. The realization of a low-voltage low-power op amp that combines high unity-gain bandwidth with desired phase margin has been a difficult problem [1], [2].

Frequency compensation is a basic step in the design procedure for op amps to ensure they remains stable and do not produce unwanted high frequency spurious oscillations. Also Frequency compensation required because stray capacitances in the chip can cause unwanted phase shifts at high frequencies. The most widely used compensation technique in op amps is pole splitting. A miller capacitor is used to split the poles, which causes the dominant pole to move to a much lower frequency and thus reducing the bandwidth and providing enough stability. The disadvantage of this technique is the Right-Half-Plane (RHP) zero created because of the direct path from the output of the first to the second stage through the compensation capacitor. This zero makes the stability of the op amp to deteriorate. Some use a resistor in series with the compensation capacitor to make the zero a left-half plane (LHP) one [3].

Different frequency compensation techniques for two stage operational amplifiers have been reported [3-9]. In [3] the authors presented a novel technique for indirect miller compensation which uses the bulk as an input to reduce the device count for creating necessary feedback signal in the indirect compensation method. In [4-7] a new frequency compensation technique which called as indirect frequency compensation for two/multi stage op amps is proposed. The indirect compensation results in much faster and low-power op amps, significant reduction in the layout size and better power supply noise rejection (PSRR). In [8] an improved frequency compensation technique which known as Ahuja compensation (cascade compensation) is presented. This technique provides stable operation for a much larger range of capacitive loads. In [9] the authors proposed a new compensation techniques based on current buffer. This technique provides high unity-gain bandwidth and better PSRR performance.

In this paper a hybrid frequency compensation technique for low-voltage low-power op amps is proposed which improves unity-gain bandwidth and phase margin and stable operation for a much larger range of capacitive loads. The organization of this paper is as follows. In section 2 and 3, the DTMOS technique and sub-threshold operation are presented, respectively. In section 4, the indirect compensation and compensation using unbalanced differential pairs are discussed. The structure of proposed op amp is described in Section 5. The simulations results are provided in Section 6 and finally the conclusion is given.

2. DTMOS TECHNIQUE

An effective method for reducing power consumption is reduction the power supply voltage. A constraint to implementing digital and analog circuits at low-voltage is the threshold voltage. The minimum supply voltage is usually required to be at least equal to [2]:

$$V_{min} = V_{th,n} + |V_{th,p}| \quad (1)$$

Where $V_{th,n}$ and $V_{th,p}$ are the threshold voltage of the n-type and of the p-type transistors respectively.

Reduction of threshold voltage is necessary for low-power low-voltage operation, so various techniques have been proposed for low-power low-voltage analog integrated circuits design [2]. DTMOS technique is the best idea for reduction threshold voltage. The DTMOS technique in 1994 (Assaderaghi et al) is proposed to overcome the drawback in a forward-biased MOSFET [10]-[12]. In DTMOS technique, the bulk is tied to its own gate as shown in Fig. 1.

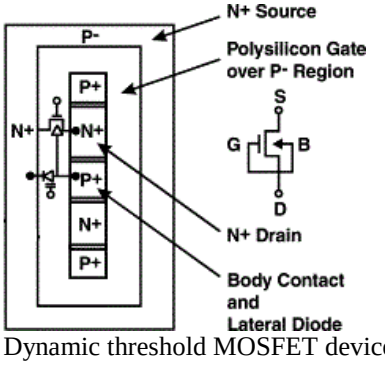


Fig. 1. Dynamic threshold MOSFET device [2].

The DTMOS technique reduces the transistor off-state leakage current and also reduces the threshold voltage during on-state ($V_{BS} > 0$) according to below equation [2]:

$$V_{th} = V_{th0} + \lambda\left(\sqrt{|2\emptyset_f - V_{BS}|} - \sqrt{|2\emptyset_f|}\right) \quad (2)$$

Where V_{BS} is the source-bulk voltage, V_{th0} the threshold voltage for $V_{BS} = 0$, λ is body effect factor with an approximate value between 0.3 to 0.4 $\sqrt{V}$, and $\emptyset_f$ is Fermi potential with a typical value in the range of 0.3- 0.4 V [2].

This technique is limited to very low supply voltage. It cannot be applied to a circuit with a supply voltage over 0.8V. To apply this technique over a wide-voltage supply range, a reverse-biased MOS diode is inserted to suppress body leakage current. However, in a large complex chip with many transistors, this leakage current would become significant [2].

3. SUB-THRESHOLD OPERATION

Operation of the MOS device in sub-threshold region is very important when low power circuits are desired. When the V_{GS} in the MOS transistor is less than the threshold voltage (V_{th}), the MOSFET works in sub-threshold region. The drain current I_D of a MOS transistor in sub-threshold region is based on the channel diffusion current and can be given by (3), when referred to source voltage [2].

$$I_D = I_S\left(\frac{W}{L}\right) exp\left(q\frac{V_{GS} - V_{th}}{nKT}\right)\left[1 - exp\left(-q\frac{V_{DS}}{KT}\right)\right] \quad (3)$$

Where I_S the characteristic current, T is the absolute temperature, n is the slope factor, K is the Boltzmann constant and q is the charge of the electron or hole. If $V_{DS} \geq 3KT/q$ then the transistor will be saturated in sub-threshold region. The transconductance g_m can be found as presented in (4), which is a function of current I_D and factor nKT/q [2].

$$g_m = q\frac{I_D}{nKT} \quad (4)$$

There is linear relationship between transconductance and current. Also transconductance is independent of device geometry. But in strong inversion relationship between transconductance and current is square law and also function of device geometry.

The body-effect transconductance g_{mb} can define as [13]:

$$g_{mb} = g_m\frac{\lambda}{2\sqrt{2\emptyset_f + V_{SB}}} \quad (5)$$

4. COMPENSATION TECHNIQUE

4.1. Indirect Compensation

In indirect compensation or indirect feedback frequency compensation, the compensation capacitor is connected to an inner low impedance node (v_x) in the first stage, which allows indirect feedback of the

compensation current from the output node to the inner high-impedance node (the output of the first stage, i.e. node (1)) [4], [7]. Fig. 2 shows a two stage op amp topology with indirect compensation.

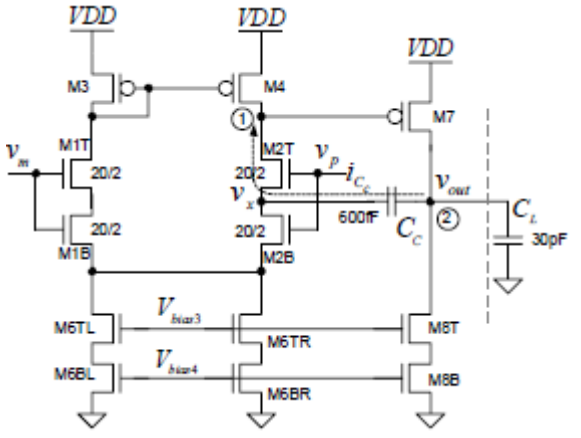


Fig. 2. Two stage op amp topology with indirect compensation [4].

The current feedback (i_{C_c}) through the compensation capacitor (C_c) can be approximated as (5) [4]:

$$i_{C_c} \approx v_{out}/(1/j\omega C_c) \tag{6}$$

In op amp with indirect compensation technique, the dominant pole location is same as in Miller compensation. While, instead of a RHP zero, the op amp have a LHP zero located at [4]:

$$f_z = \frac{g_{mc}}{2\pi(C_c + C_{v_x})} \tag{7}$$

Where g_{mc} is the transconductance of the common-gate amplifier and C_{v_x} is the capacitance connected to the low impedance node (v_x).

4.2. Compensation Technique using Unbalanced Differential Ppairs

This technique is based on "multi-tanh" principle. The "multi-tanh" principle refers to a group of linear transconductance cells, specified by the use of parallel- or series-connected sets of differential pairs. The multi-tanh principle is suitable for low-voltage operation and increase bandwidth of the op amp [14].

In Fig. 2 the aspect ratio of M_1 is n times that of M_2. This mismatch can be achieved by scaling either the width or length of the input pair [14]. If n = 1, the differential input pair is balanced and if n ≠ 1, then the differential input pair is unbalanced. For the unbalanced differential pair, output current i_o is given by [14]:

$$i_o = i_1 - i_2 \tag{8}$$
$$= \left(\frac{n-1}{n+1}\right) I - 2\gamma k v_i^2 + \frac{\alpha}{\sqrt{n+1}} \sqrt{kI} v_i \sqrt{1 - \alpha \frac{k}{I}\left(\frac{v_i}{2}\right)^2}$$

Where i_1 and i_2 are the drain currents of transistors M_1 and M_2 respectively, k is the transconductance parameter, α and γ are defined as [14]:

$$\alpha = 4\frac{n}{n+1} \tag{9}$$
$$\gamma = \frac{n}{(n+1)^2}(n-1) \tag{10}$$

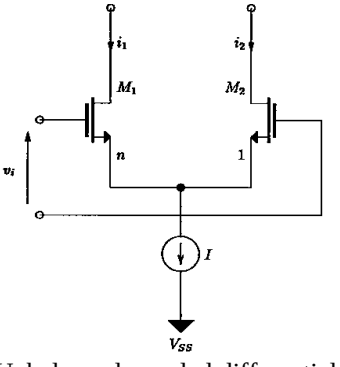


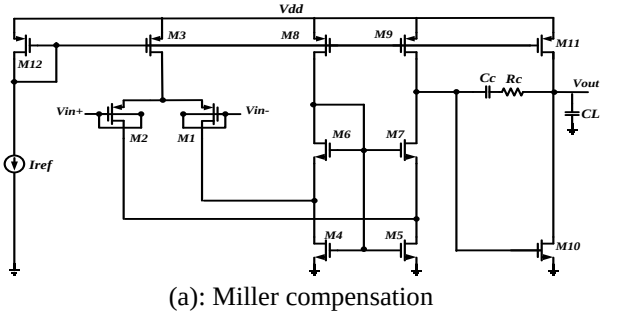
Fig. 3. Unbalanced coupled differential pair [14].

According to equation (8), if the applied voltage to the differential input pair is zero ($v_i = 0$), output current of $((n-1)/(n+1))I$ flows in an unbalanced differential pair. In a balanced differential pair, under the same operating conditions, the drain current of the input pair transistors are the equal, and as a result, the differential output current is zero [14].

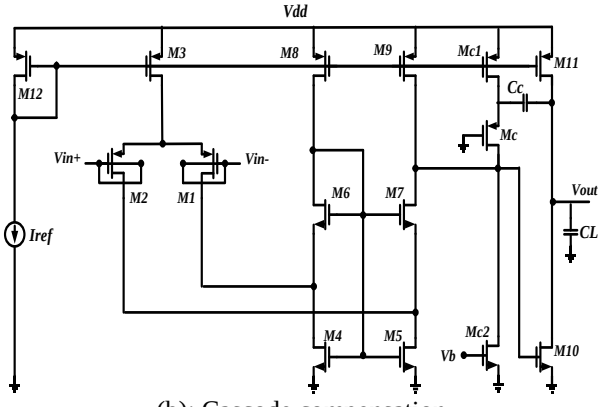
5. CIRCUIT DESCRIPTION

5.1. Comparison of Miller, Cascode and Indirect Compensation

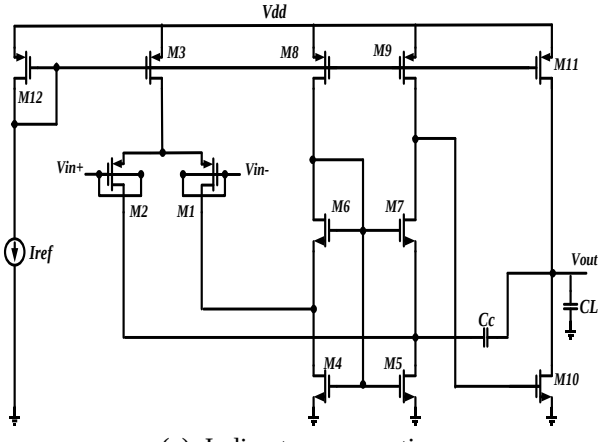
The two stage operational amplifier circuit shown in Fig. 3 is used to compare the Miller, cascode and indirect compensation. The DTMOS technique is used in the differential input pair and all transistors are biased in the sub-threshold region.



(a): Miller compensation



(b): Cascode compensation



(c): Indirect compensation

Fig. 4. Two stage operational amplifier.

5.1.1. Circuit analysis

The AC small signal equivalent circuit for the op amp using Miller compensation is shown in Fig. 4. g_{oi} is the output conductance of M_i transistor and $g_{oi,j}$ shows parallel conductance of M_i and M_j transistors. Also, C_{n1} and C_{n2} are the parasitic capacitances between the source and drain nodes of transistor M_7. g_m, g_{mb} and g_o are obtained from DC biasing conditions [15].

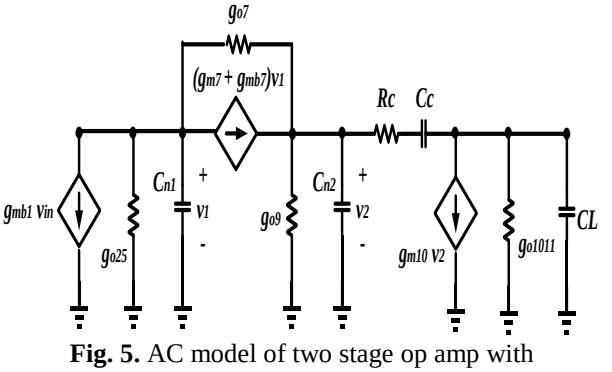


Fig. 5. AC model of two stage op amp with Miller compensation [15].

The open loop gain is given by [15]:

$$A_0 = \frac{g_{mb1}g_{m10}}{g_{o1011}\left(\frac{g_{o7}+g_{o9}}{g_{m7}+g_{mb7}+g_{o7}}g_{o25}+g_{o9}\right)} \quad (11)$$

The dominant pole f_d, non-dominant pole f_n and zero f_z are obtained from the following equations [15]:

$$f_d \approx -\frac{g_{mb1}}{2\pi A_0 C_c} \quad (12)$$

$$f_n = -\frac{g_{m6}}{2\pi C_L} \quad (13)$$

$$f_z = -\frac{1}{2\pi C_c\left(R_c - \frac{1}{g_{m6}}\right)} \quad (14)$$

5.1.2. Simulation results

The presented op amps in Fig. 3 are simulated in HSPICE software with 0.6 power supply in TSMC 0.18μm 1P6M CMOS technology. The size of each transistor, capacitors and other parameters are shown in Table 1.

Table 1. Size of transistors, capacitors and other parameters.

M1-M2	(W/L) 90um/0.18um
M3	(W/L) 200um/0.18um
M4-M5	(W/L) 2um/0.18um
M6-M7	(W/L) 25um/0.18um
M8-M9	(W/L) 80um/0.18um
M10	(W/L) 1um/0.18um
M11	(W/L) 100um/0.18um
M12	(W/L) 70um/0.18um
Miller Compensation	Cc=10 pF, Rc=10 kΩ
Cascode Compensation	Cc=2 pF, I1=I2=0.5 nA Mc (W/L) 0.5um/0.2um
Indirect Compensation	Cc=3 pF
Load Capacitance	CL=15 pF
Reference current	Iref =20 nA

Typical op amp performances such as power consumption, open loop gain, phase margin and unity-gain bandwidth have been simulated at TT corner and temperature 27°C. Simulation results for AC analysis for gain and phase plot vs. frequency is shown in Fig. 5.

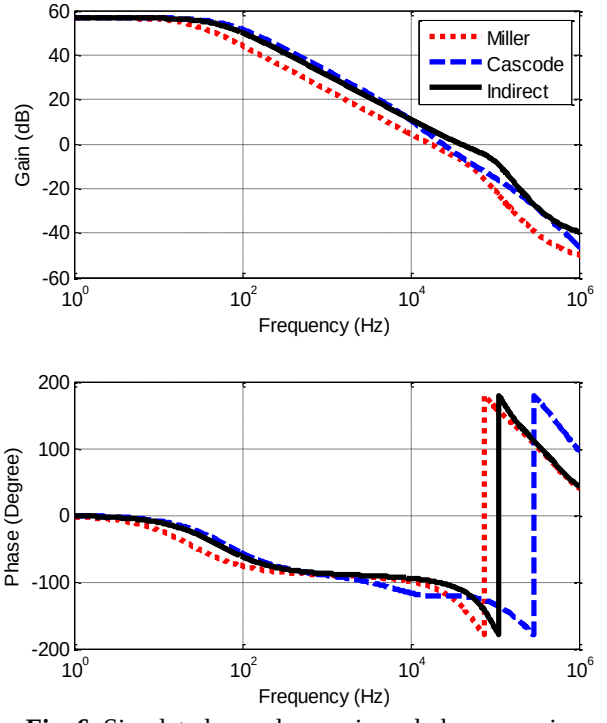


Fig. 6. Simulated open loop gain and phase margin.

A summary of simulation results is presented in Table 2. By using indirect compensation technique, unity-gain bandwidth has increased 130% and 62%, respectively, than Miller and cascade compensation techniques. Also, indirect compensation requires a smaller compensating capacitor than Miller compensation and, on the other hand, has a smaller layout than cascode compensation.

Table 2. Summary of simulation results.

	Indirect	**Cascode**	**Miller**
Gain (dB)	56.62	56.62	56.62
Phase margin (Deg.)	68.8	58.2	73.2
UGBW (kHz)	38.9	24	16.9
Power consumption (nW)	86.82	87.12	86.82

5.2. Hybrid Frequency Compensation to Improve Unity-gain Bandwidth

The proposed two stage op amp shown in Fig. 6, indirect compensation and compensation using unbalanced differential pairs is used to increase bandwidth. In this design, three unbalanced differential inputs with DTMOS technique have been used and all transistors operation in sub-threshold region.

Differential output current (i_o) is given by [14]:

$$i_o = i_{157} - i_{248} = \cdots = \sqrt{2kI}v_i\sqrt{1-\frac{k}{I}\frac{{v_i}^2}{2}} + \frac{2\alpha}{\sqrt{n+1}}\sqrt{kI}v_i\sqrt{1-\alpha\frac{k}{I}\left(\frac{v_i}{2}\right)^2} \quad (15)$$

Where i_{157} and i_{248} are the drain currents of transistors $M_{1,5,7}$ and $M_{2,4,8}$ respectively.

Small signal transconductance is given by [14]:

$$g_m = \cdots = \sqrt{2kI}\left[\frac{1-\frac{k}{I}{v_i}^2}{\sqrt{1-\frac{k}{I}\frac{{v_i}^2}{2}}}\right] + \frac{2\alpha}{\sqrt{n+1}}\sqrt{kI}\left[\frac{1-\alpha\frac{k}{I}\frac{{v_i}^2}{2}}{\sqrt{1-\alpha\frac{k}{I}\left(\frac{v_i}{2}\right)^2}}\right] \quad (16)$$

The DC gain of the proposed amplifier approximately is:

$$A_0 = \cdots = \frac{g_{mb7}g_{m17}}{g_{o16,17}\left(\frac{g_{o12}+g_{o14}}{g_{m12}+g_{mb12}+g_{o12}}g_{o2,11}+g_{o14}\right)} \quad (17)$$

The size of each transistor, capacitors and other parameters are shown in Table 3.

Table 3. Size of transistors, capacitors and other parameters.

M1, M4, M5, M8	(W/L) 50um/0.18um
M2, M7	(W/L) 40um/0.18um
M3, M6, M9	(W/L) 72um/0.18um
M10, M11	(W/L) 2um/0.18um
M12, M13	(W/L) 25/0.18um
M14, M15, M18	(W/L) 80um/0.18um
M16	(W/L) 100um/0.18um
M17	(W/L) 1um/0.18um
Compensation Capacitance	Cc=3.5 pF
Load Capacitance	CL=15 pF
Reference current	Iref=10 nA

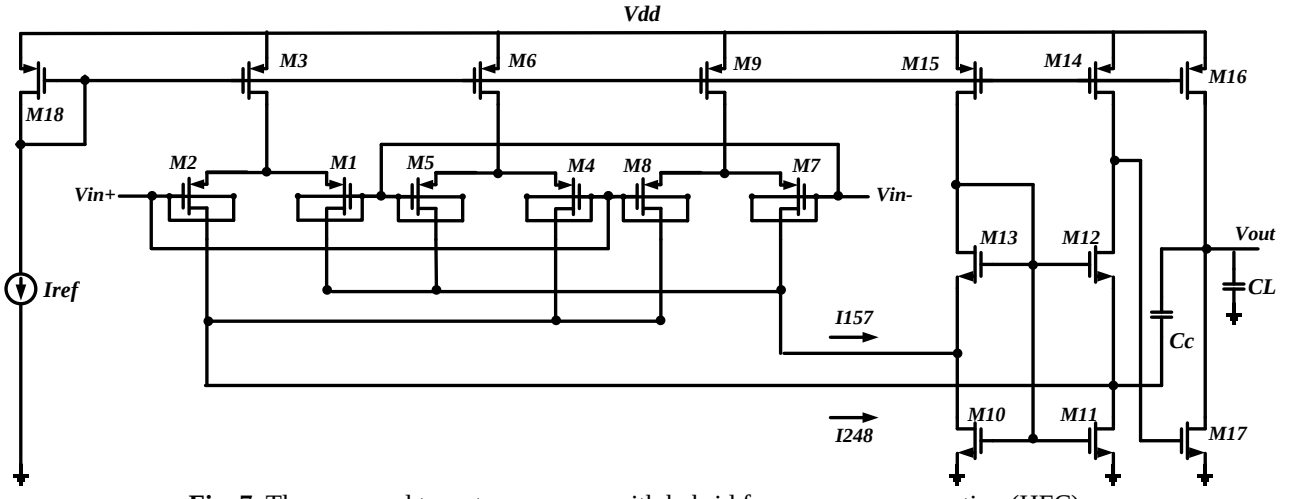


Fig. 7. The proposed two stage op amp with hybrid frequency compensation (HFC).

6. SIMULATION RESULTS

The proposed op amp is simulated in HSPICE software with 0.6 power supply in TSMC 0.18µm 1P6M CMOS technology. The simulated open loop gain and phase margin are shown in Fig. 7. The simulation result shows the open loop gain is 58.59 dB, the unity gain-bandwidth is 81.28 kHz, phase margin is 60.7 degree and power consumption is 138.3 nW. Also the input referred noise is 5.537 $\mu V/\sqrt{Hz}$ @ 100 Hz and the CMRR is 69.49 dB @ 10 Hz.

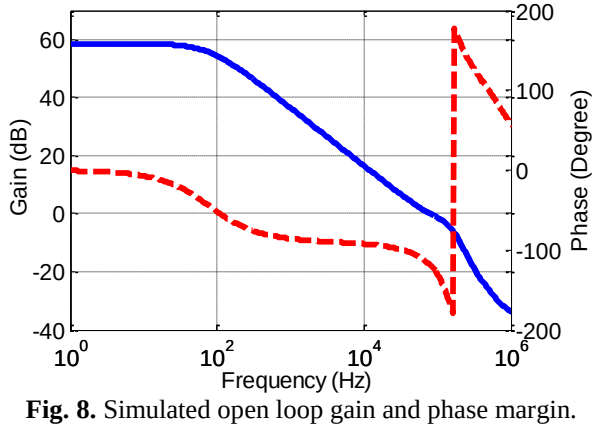


Fig. 8. Simulated open loop gain and phase margin.

The effect of supply voltage variation on open loop gain and phase margin is shown in Fig. 8. According to this figure, the designed circuit has the same performance as the supply voltage variation.

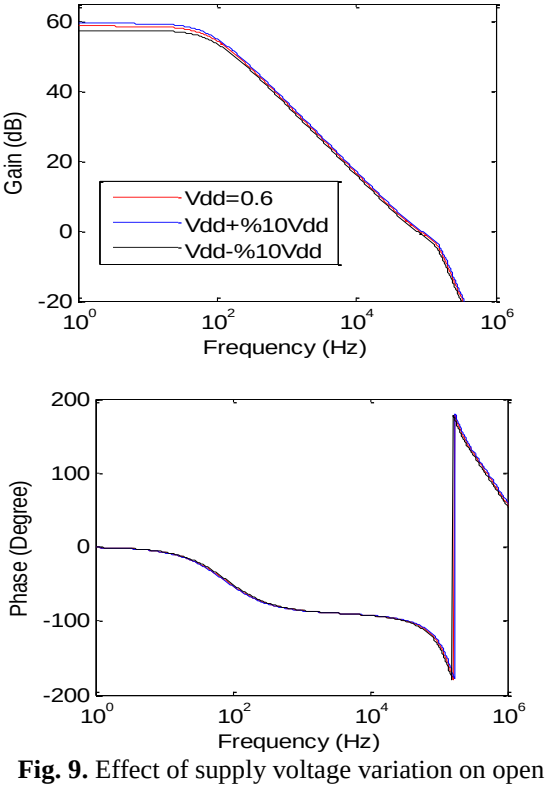


Fig. 9. Effect of supply voltage variation on open loop gain and phase margin.

In Fig. 9, open loop gain and phase margin are shown in three different temperatures and three different corners.

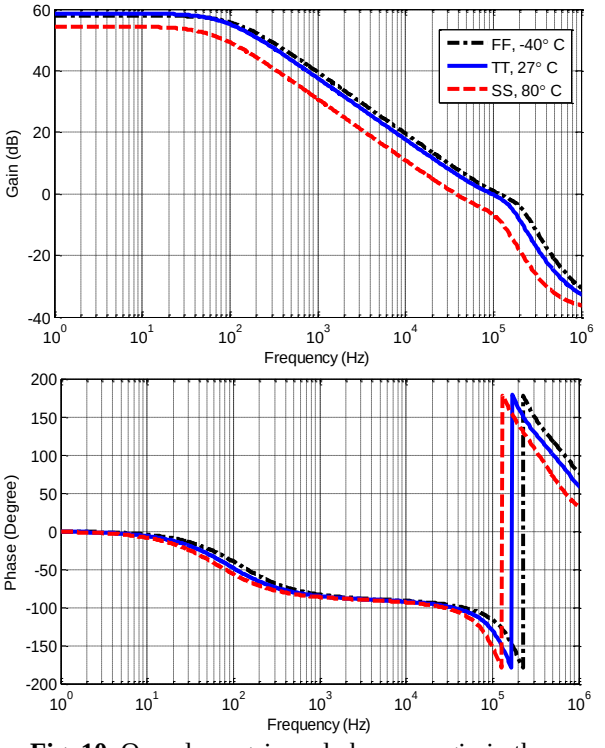


Fig. 10. Open loop gain and phase margin in three different temperatures and three different corners.

In Table 4, the proposed op amp with HFC compensation is compared with other operational amplifiers which used different compensation technique. To evaluate this work a figure of merit (FOM) can be defined as:

$$FoM = \frac{Gain\ (dB) * UGBW\ (kHz)}{Power\ supply\ (mV) * Power\ consumption\ (\mu W) * Cc\ (pF)} \quad (18)$$

7. CONCULSION

In this paper a low-voltage low-power two stage op amp with hybrid frequency compensation is designed and simulated. This proposed compensation utilizes indirect compensation and compensation using unbalanced differential pairs. Also to reduce power consumption and use low supply voltage, DTMOS technique and sub-threshold region are employed. Simulation results have been presented to confirm the considerable improvement in unity-gain bandwidth. The op amp operate at 0.6 V power supply with 138.3 nW power consumption. The simulation result shows the open loop gain is 58.59 dB, the unity gain-bandwidth is 81.28 kHz and phase margin is 60.7 degree. Also, the output voltage swing is 0-0.52 V. The proposed op amp shows a considerable FOM than other op amps.

Table 4. Comparison proposed op amp with other op amps.

	Proposed	**[13]**	**[16]**	**[17]**
Technology (µm)	0.18	0.18	0.13	0.18
Power supply (mV)	600	400	250	600
Power consumption (µW)	0.1383	0.386	0.018	0.396
Gain (dB)	58.59	91	60	82
Phase margin (Degree)	60.7	66	52.5	55
UGBW (kHz)	81.28	111.4	1.88	17.7
CMRR (dB)	69.49 @ 10 Hz	106	N/A	N/A
PSRR (dB)	78.65 @ 10 Hz	N/A	N/A	N/A
Slew Rate (V/µs)	5.375	0.022	0.00064	N/A
Output voltage swing (V)	0-0.52	N/A	0.24	600
Input referred noise ($\mu V/\sqrt{Hz}$)	5.537 @ 100 Hz	0.01 @ 10 mHz	3.3	4.39 @ 1 Hz
C_C (pF)	3.5	5	5	5
C_{Load} (pF)	15	15	15	15
FOM ($dB.kHz$)/($mV.\mu W.pF$)	16.4	13.13	5.01	1.222

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