A High-Speed High-Input Range Four Quadrant Analog Multiplier

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Received: August 2009 Revised: October 2009 Accepted: December 2009

ABSTRACT:
In this paper, a CMOS four quadrant multiplier based on flipped voltage follower and differential squaring circuit is presented. The proposed circuit has a compact architecture which operates at a higher speed and a higher input voltage range compared to the previously presented structures. The transistors operate in both saturation and ohmic regions. The circuit operates with a single supply voltage of 3.3V in a 0.35 µm CMOS technology where the total harmonic distortion (THD) is less than 1.1%, the linearity error is also less than 3%, -3db frequency is more than 180 MHz and the voltage input range is $3V_{p-p}$. Simulation results are given to verify the functionality of the proposed multiplier.

KEYWORDS: Analog Multiplier, Four Quadrant Multiplier, Defuzzification, CMOS.

1. INTRODUCTION

The multiplier circuit is a very useful and important subcircuit in many applications such as analog signal processing, fuzzy logic controllers (FLC), analog filtering, frequency doublers, and modulators. Its intent is to perform a linear product of two continues signals x and y, yielding an output of $Z = K \cdot X \times Y$ where K is constant with a suitable dimension. In this paper, we present a new multiplier with emphasis on the speed and value of the input voltage range. We analyze various performance metrics of the multiplier and provide some design considerations. It has been demonstrated in particular that this multiplier performs much better than other structures such as [2, 3, 5] in terms of the speed and input range. This multiplier is proposed of the multiplier circuit that uses quarter-square algebraic identity techniques. It consists of four input blocks and squaring transistors.

The paper is organized as follows, section 2 presents the multiplier circuit and its analytical formulas, section 3 gives an application of the proposed circuit, and section 4 gives some experimental results, and finally section 5 concludes the paper.

2. QUARTER-SQUARE MULTIPLIER

The differential squaring circuit is illustrated in Fig. 1. One of the input voltages is applied to the gates (x) and the other one to the sources (y) of transistors M1-M4 which are biased with appropriate common-mode voltages X and Y in saturation region. Therefore the drain current of each transistors can be calculated by equation (1).

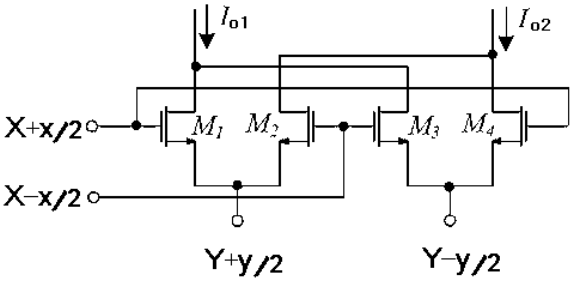

Fig. 1. The multiplier using differential squaring circuit

$$I_d = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)\left[V_{GS} - V_{TH}\right]^2 \quad (1)$$

Where V_{TH} is the threshold voltage of NMOS transistors, the differential output current of the circuit proportional to the multiplication of two input signals is calculated in equations 2 and 3.

$$I_O = (I_{d1} + I_{d3}) - (I_{d2} + I_{d4}) = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right) \times 2 \times xy \quad (2)$$

$$I_O = \mu C_{ox}\left(\frac{W}{L}\right)xy \quad (3)$$

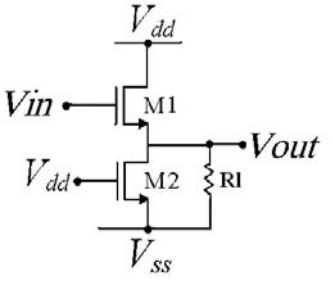

Fig. 2. The input block of multiplier circuit

When the attenuator circuit is used as the X input of the multiplier, the voltage level shifter has to be used at the output of attenuator circuit; the resulted attenuator circuit is presented in fig. 3.

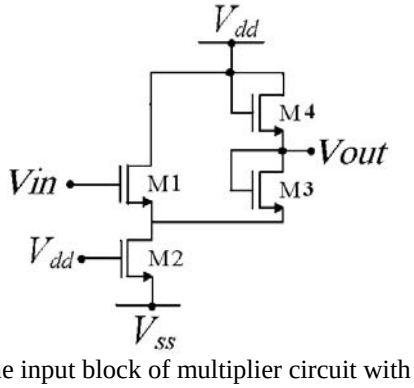

Fig. 3. The input block of multiplier circuit with voltage level shifter

As transistor M1 works in the saturation region the output voltage of that circuit can be written as

$$V_{out} = \frac{\frac{1}{g_{mb}} \| r_{o1} \| r_{o2} \| R_L}{\frac{1}{g_{mb}} \| r_{o1} \| r_{o2} \| R_L + \frac{1}{g_m}} \times V_{in} \quad (4)$$

So the gain of attenuator circuit can be calculated as

$$A_v = \frac{V_{out}}{V_{in}} = \frac{\frac{1}{g_{mb}} \| r_{o1} \| r_{o2} \| R_L}{\frac{1}{g_{mb}} \| r_{o1} \| r_{o2} \| R_L + \frac{1}{g_m}} \quad (5)$$

In above equations $R_L \cong \frac{1}{g_m}$ and $A_V < 1$. In this way both input-signals are attenuated before being applied to the multiplier inputs. With regard to the above principle a wide-range and high-speed analog multiplier can be completely constructed as illustrated in Fig. 4.

3. AN APPLICATION OF PROPOSED CIRCUIT

To illustrate the application of this multiplier, the circuit has been used in a defuzzifier block of a fuzzy logic controller (FLC). A number of defuzzification strategies exist, each with its own advantages and drawbacks. The center of area (COA) method is the most common defuzzification method, also known as "Center of Gravity" or "Centroid" method. Method's Equation is shown in Eq. (6).

$$V_o = \frac{\sum Y_i X_i}{\sum X_i} \quad (6)$$

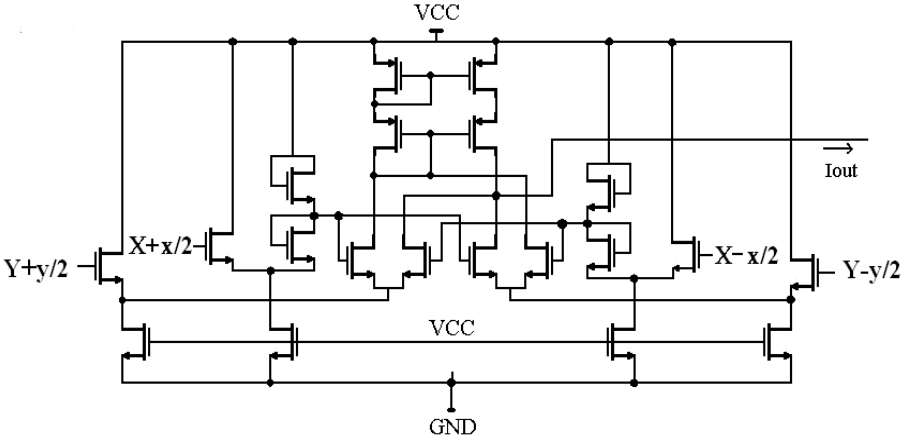

Fig. 4. The complete of wide-range analog multiplier circuit

As illustrated in Eq. (6) this method of defuzzification needs a divider. The used divider circuit is shown in Fig. 5 [6]

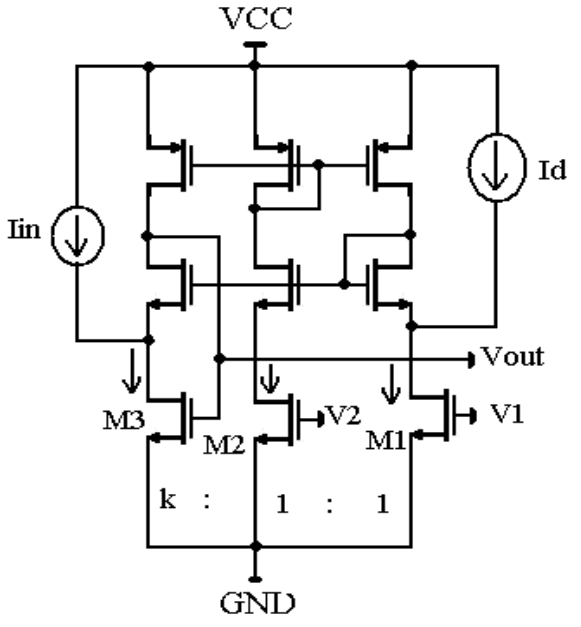

Fig. 5. The referenced divider circuit

The division is performed by means of transistors M1, M2, M3, all of them being constrained to operate in the triode region. While V1 and V2 are fixed bias voltages, the following relations hold for the drain currents of the triode transistors [6]:

$$I_1 = \beta V_{ds}\left(V_1 - V_{TN} - \frac{n}{2}V_{ds}\right) = I_d + I_2 \quad (7)$$

$$I_2 = \beta V_{ds}\left(V_2 - V_{TN} - \frac{n}{2}V_{ds}\right) \quad (8)$$

$$I_3 = k\beta V_{ds}\left(V_{out} - V_{TN} - \frac{n}{2}V_{ds}\right) = I_{in} + kI_2 \quad (9)$$

Where Vds is the common drain-to-source voltage drop for the three bottom transistors and β is the current gain ratio of M1 and M2. Therefore from the three equations (7 - 9) the output equation of divider can be written as:

$$\left(V_{out} - V_2\right) = \frac{\left(V_1 - V_2\right)}{k}\frac{I_{in}}{I_d} \quad (10)$$

In the block diagram of the defuzzifier shown in Fig. 6., two input voltages X and Y have been applied to the multiplier and the summation of output currents of multipliers has been applied to the divider.The other input of divider is the summation of Xs as shown in Eq. 6, where X is output of rule-base and Y is singleton.

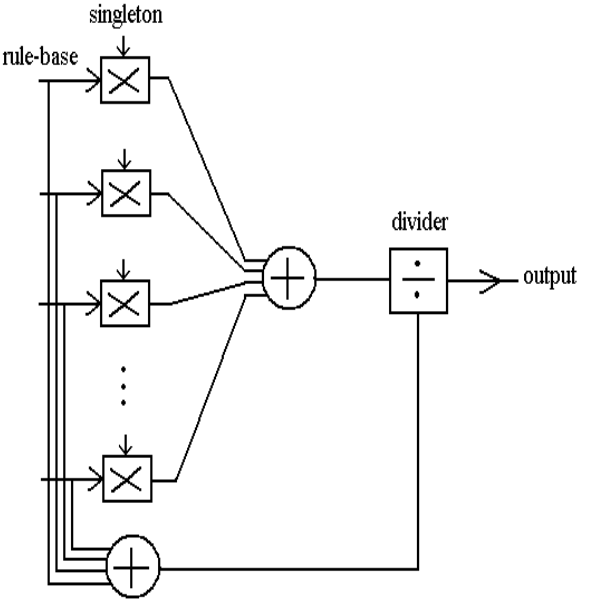

Fig. 6. Block diagram of defuzzifier

4. THE SIMULATION RESULTS

The proposed multiplier has been simulated using Hspice and level 49 BSIM3V3 parameters. The circuit operates with a single supply voltage of 3.3V in a 0.35 µm CMOS technology. The DC-characteristic of the multiplier is shown in Fig. 7. The resulting Vxs for different discrete Vy values varying from -1.5V to +1.5V is shown on the x-axis. Whereas in Fig. 8. Vy values for different values of Vx come in the x-axis.

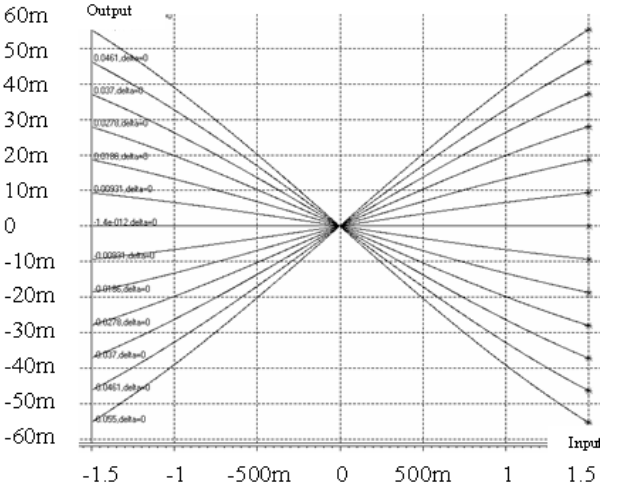

Fig. 7. DC-characteristic of proposed circuit for Vx in x-axis

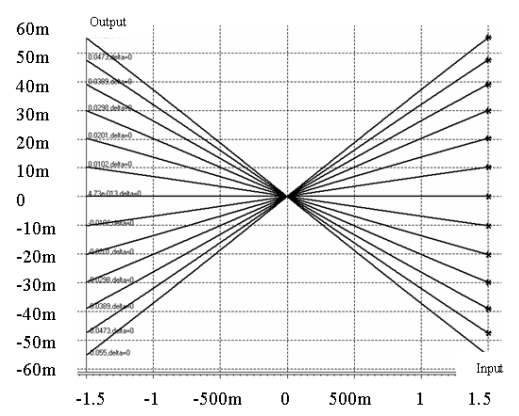

Fig. 8. DC-characteristic of proposed circuit for Vy in x-axis

The frequency response of the proposed circuit for constant values of X is shown in Fig. 9. The band width is more than 180 MHz and vice versa and the frequency response for constant values of y, is shown in Fig. 10.

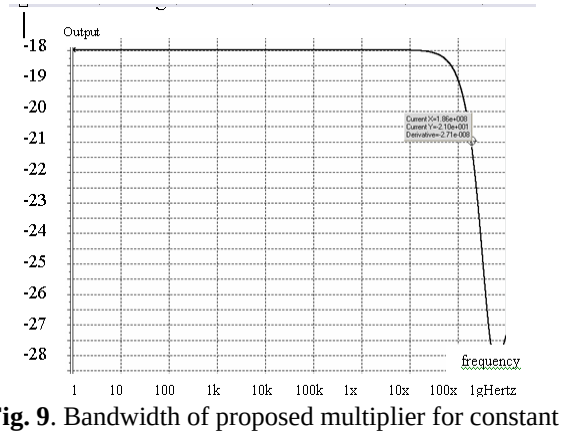

Fig. 9. Bandwidth of proposed multiplier for constant values of x

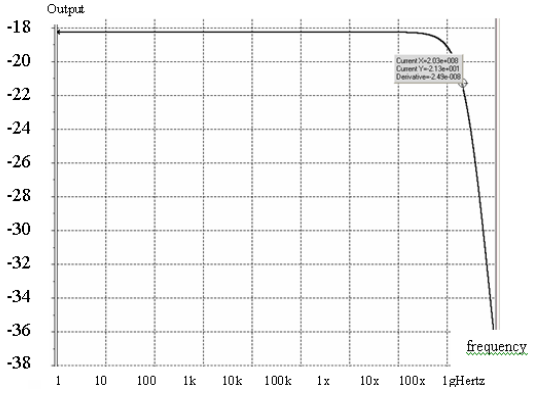

Fig. 10. Bandwidth of proposed multiplier for constant values of y

As a common application, the multiplier was used as an amplitude modulator. (The amplitude modulation is used to confirm as an application)→ I don't get this! The frequencies of the inputs Vx and Vy are 10MHz and 1MHz, respectively. The amplitude of both inputs is 2Vp-p. The input signals and AM output signal are shown in Fig. 11.

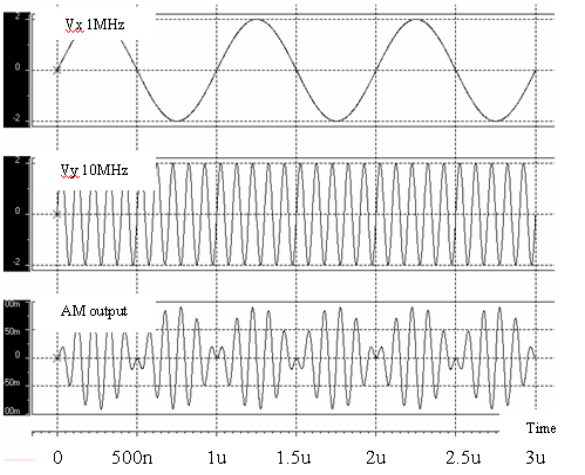

Fig. 11. The AM output signal while input is 10MHz and 1MHz (Vx (top), Vy (middle) and AM output (bottom))

The linearity error over input Vx is also illustrated in Fig. 12 for fixed (given) voltages of Vy. It can be shown that the maximum value for linearity error is less than 3%.

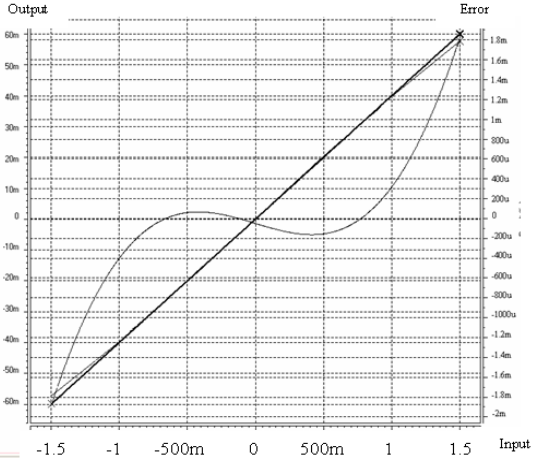

Fig. 12. The linearity error of the proposed circuit

The total harmonic distortion (THD) has also been considered. The 1 MHz frequency has been applied for input Vy with amplitude of $2V_{P-P}$ while the other input Vx takes different discrete values. The THD result is shown in Fig. 13 that is less than 1.1%.

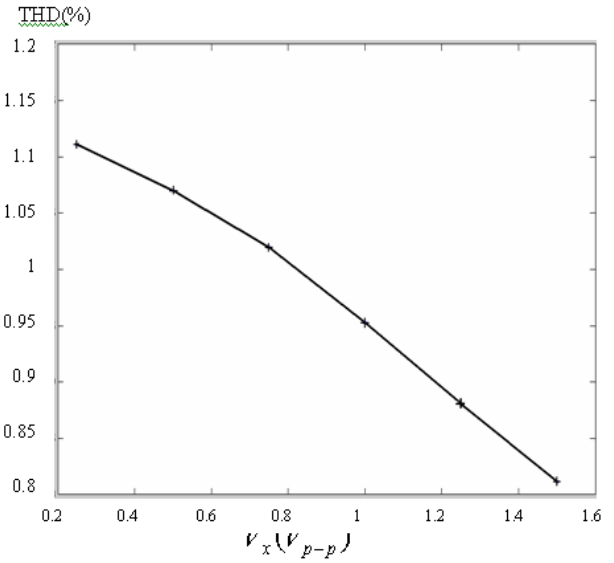

Fig. 13. the THD of the proposed circuit

5. CONCLUSIONS

A new CMOS voltage-mode four-quadrant multiplier based on the square-law characteristic of MOS transistors has been presented that achieves an output signal in current form without using resistors. The multiplier achieves this goal with about 3% linearity error. The total harmonic distortion is less than 1.1% and the -3dB bandwidth is 180MHz. The performances have been demonstrated using HSPICE simulations.

Table 1. Comparison between the proposed circuit and some recently reported multipliers

Circuit	Input range	THD	-3dB frequency
This work	±1.5V	1.1%	180Mhz
[2]	±1.5V	0.7%	141Mhz
[3]	±500mV	0.76%	35Mhz
[7]	±1V	0.9%	200Khz
[8]	500mv	1.1%	2.2Mhz
[9]	not indicated	1.5%	12.3Mhz
[10]	±200mV	1.63%	10Mhz

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