

Design and Analysis of Three New SRAM Cells

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ABSTRACT:

Three new SRAM cells are proposed in this paper. Increasing area overhead is the major concern in SRAM design. One of the new structures is included four transistors instead of six transistors as it is used in conventional 6T-SRAM cell for very high density embedded SRAM applications. The structure of proposed SRAM employs one word-line and one bit-line during Read/Write operation. The new SRAM cell has smaller size, leakage current and power dissipation in contrast of a conventional six transistor SRAMs. A proposed 4T-SRAM cell has been simulated for 256 cells per bit-line and 128 columns cell for supply voltage of 1.2V. Furthermore, two other new structures are included 10 and 11 transistors. These new structures have been separate read and write process by changing in the structure of conventional 6T SRAM to achieve high Static Noise Margin (SNM). Using 10T and 11T SRAM cells lead to apply 512 cells per bit-line by reducing leakage current technique, while the cell is unavailable. 128 columns cell array has been built to measure the operation of SRAM cell. To have low power dissipation, the supply voltage for 10T and 11T are chosen 0.32V and 0.27V, respectively. Proposed SRAM uses one read bit-line during read operation. Simulation results have been confirmed by HSPICE in 0.13um process.

KEYWORDS: SRAM, Static Noise Margin (SNM), Power, Access time, Leakage current.

1. INTRODUCTION

As electronics continues to be integrated into portable consumer devices, the demand grows not only for increased functionality, but also for long battery life and small physical size [1]. Building a memory cell which has the same efficiency in both Reading and Writing, needs a complicated structure. To save something in RAM happens by feedback or the capacitor's load [2]. The memory cell must be designed in a way to give the most signals in the least size. Static Random Access Memory (SRAM) continues to be one of the most fundamental and vitally important memory technologies today. Because they are fast, robust, and easily manufactured in standard logic processes, they are nearly universally found on the same die with microcontrollers and microprocessors [3]. A six-transistor SRAM cell (6T SRAM cell) is conventionally used as the memory cell. Reducing the number of transistors in the basic cell leads to reduce the number of transistors in the SRAM array and consequently decreasing chip's area. This paper proposed 4T-SRAM cell to reduce area and power consumption.

Ultra low voltage in sub-threshold range for operation of memory cells has become a topic of much

interest due to its applications in very low energy computing and communications [4]. Reducing the power supply voltages to the sub-threshold region is one of the effective approaches for ultra low-power applications. Operating memory circuits at such a low voltage is more challenging since SRAM yield degrades considerably at these low voltages. There are several challenges when the supply voltage is scaled down to the sub-threshold region, including: (i) reduced the stability of cells; (ii) reduced number of cells per bit-line and (iii) bit-line sense margin problem [5]. To solve this problem, many researchers have proposed different structures. The cost of these improvements was added some transistor to the conventional of 6T SRAM. An 8-T cell with a 2-T read buffer was shown to be functional in the near sub-threshold regime in [5], [6]. The extra transistors isolate memory cells from the read bit-line to improve read stability and decouple them read and write requirements. The maximum number of cells per bit-line in the 8T sub-threshold SRAMs was limited to 256 at 0.35V. The authors of [7] proposed a 10-T cell with a 4-transistor read buffer that remained functional with the supply voltage as low as 200 mV to make the better read SNM and the maximum number of cell per bit-line in this structure

was limited to 1024. The authors of [7] and [8] have proposed two different structures to keep the node read data high; to prevent the leakage current. This paper introduced two new structures for designing high density SRAM in the sub-threshold. These structures consist of 10 and 11 transistors to solve the problem of conventional 6T-SRAM cell.

This paper is organized as follows. A conventional 6T-SRAM cell with simulation results are presented in section 2. In section 3, the structure of proposed 4T-SRAM cell is shown. A new 10T-SRAM cell with simulation results have been presented in section 4. Finally, section 5 and 6 show 11T-SRAM cell with simulation results and conclusion, respectively.

2. A CONVENTIONAL 6T-SRAM CELL

The conventional six transistors (6T) structure is shown in Figure 1. A 6T SRAM cell consists of two cross-coupled inverters (M1-M3 and M2-M4). M1 and M2 are drive transistors and M3 and M4 are the load transistors and the access transistors consist of M5 and M6.

The gate terminals of both access transistors are connected to the word-line (WL) to perform write operations and the read operations through the column bit lines (BL & BLB). Bit-lines are used to connect SRAM cells to sense-amplifier during read operations and to write circuitry during write operation. The dual bit lines are used to improve noise margins over a single bit line. The 6T SRAM cell can not work in the sub-threshold region because of reducing signal levels and increasing variation. In this structure, read and write operation depends on strengths of transistors. For the write margin characterizes the ability of the access devices to over-power the load devices. Figure 1 (b) presents the variation of write margin operation versus power supply voltage. For the read static noise margin the driver transistor is stronger than the access transistor as shown in Figure 1 (c). Additionally, the hold SNM depends on the structure of cross coupled inverters as shown in Figure 1 (d).

One of the important challenges in the 6T SRAM is bit-line leakage. The small $I_{on}-I_{off}$ ratio in the sub-threshold region limits the number of cells per bit-line. The total bit-line leakage current of an SRAM memory depends on three main factors: (i) the number of cells in a bit-line column; (ii) the data stored in the cells (0 or 1) and (iii) the characteristics of the access transistors. Figure 2 (a) shows the read current on one pair of bit-lines [5].

3. A NEW 4T-SRAM CELL

A 4T SRAM cell is shown in Figure 2. The implemented circuit consists of 4 transistors instead of 6 transistors as in conventional SRAM cell.

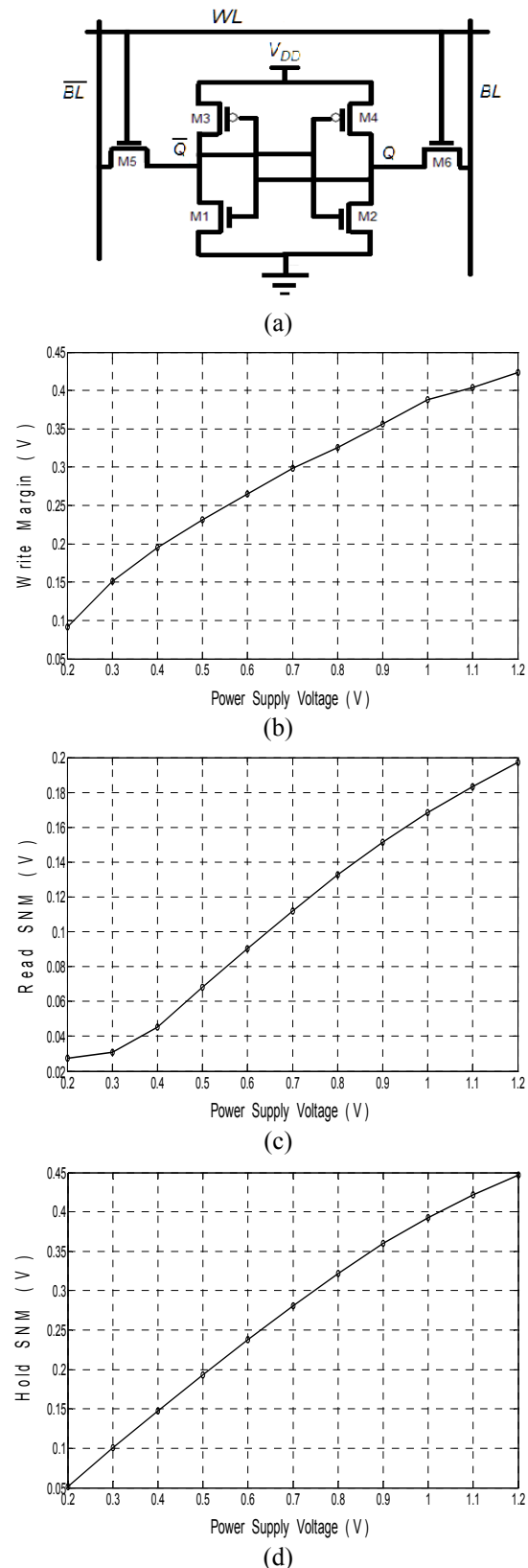


Fig. 1. (a) Conventional 6T-SRAM cell. (b) Write SNM. (c) Read SNM. (d) Hold SNM.

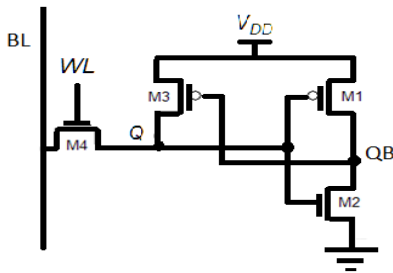


Fig. 2. A new 4T-SRAM cell

Due to lower power dissipation of the 4T SRAM cell, the area is smaller than conventional 6T SRAM cell. The circuit consists of an inverter along with an access transistor (M4) which is controlled by the word line (WL) for read and write operation and load transistor (M3) which is controlled by the QB for feedback operation. The process of read and write operation are described in below.

When reading is processed, the following order must be established in memory cell:

- 1- The BLB should be precharged and then should be separated. In this structure precharged is connected to VDD.
- 2- Then the WL must be activated that these two circumstances may happen:
 - A- When the Q node is down, BL voltage may come down.
 - B- When the Q node is up, BL voltage may go up.
- 3- Amplifier is turned on to read data on BL. This cell uses sense amplifier which is shown in Figure 3. The circuit of the sense amplifier is the same as inverter.
- 4- At the end of Reading process, the cell must go to stand-by mode, so the WL must be reset to zero.

It should be noted that the 4T-SRAM circuit only has an existing one BL and data get from Q, so one inverter to sense in order to get Q data is used.

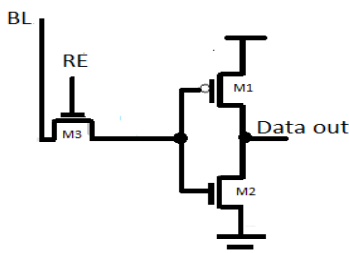


Fig. 3. Sense amplifier of a new 4T-SRAM cell

When writing is processed the following order must be established in memory cell:

- 1- At the first, the data must be put in BL and WL should be connected to VDD.
 - A- If the data is Zero, here the exiting Q is got down by M4.
 - B- If the data is one, here the exiting Q is got up by M3.

- 2- At the end of writing process, the cell must wait for the next mode; therefore, WL is connected to GND and BL connected to VDD.

It should be noted that the 4T-SRAM circuit asserted to BL.

3.1. Leakage Current of 4T-SRAM Cell

In this paper, we compare leakage current of the 6T SRAM cell and proposed 4T SRAM cell when the cell is out of access. The small $I_{on-to-I_{off}}$ ratio in the memory of SRAM cell limits the number of cells per BL and negatively impacts the SRAM density. As the number of cells in a BL increase, BL leakage from the unaccessed cells can rival the read current of the accessed cell making it difficult to distinguish between the BL high and low levels [5]. We calculated leakage current of unaccessed transistor, (I_{SD-M4} in Figure 1). In the Figure 2, BL asserted to VDD and WL of the cell asserted to GND. As shown in Figure 4, leakage current in the SRAM cell depends on data stored in the Q and QB. For example, if node QB is high and node Q is low, the leakage current is less when the node QB is low and node Q is high, since QB node is high. Table.1 shows this result for leakage current of the 6T SRAM cell and proposed 4T SRAM. The proposed 4T SRAM cell has lower leakage current than 6T SRAM cell. It is concluded in the novel SRAM cell, the number of cells per bit-line is increased than the conventional 6T SRAM cell. So, the read current must be much higher than the worst case aggregate leakage current.

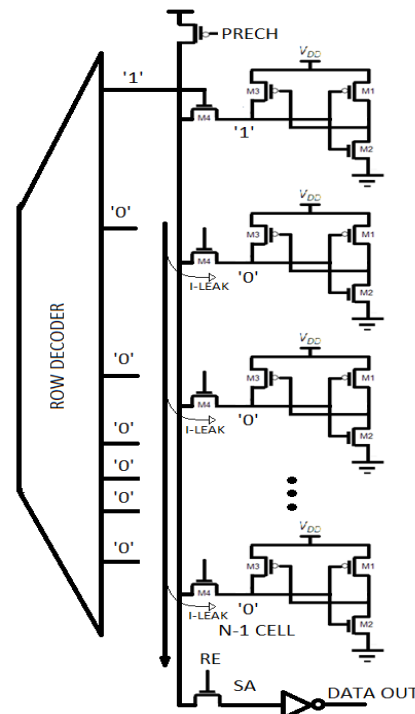


Fig. 4. Leakage current

3.2. Access time and Power

In this section, we will describe the two main performance parameters of the BL column, namely the access time and active energy consumption. The read access time is a very important performance parameter of the bit-line column and therefore we investigate the interaction between the SRAM cells and sense amplifier. During the read operation of a memory cell, the access time is proportional to the time required to create a voltage from the BL which is large enough to obtain a correct sense amplifier output. The read current of the cell discharges of the BL to generate the required voltage [9]. However, in worst-case situation, all other inactive cells in the BL column will have an opposite content with respect to the active cell and their leakage currents will discharge the BL, affecting the access time (Figure 4).

As shown in Figure 5 (a), a low VDD causes a low read current, resulting in a high read delay. This Figure showed read access time for this SRAM array under different values of power supply voltage in 130 nm CMOS technology for 128 and 256 cells per BLB at 298K temperature. As shown in Fig. 4 (a), if the numbers of cell per BL are increasing, resulting in a high Taccess. In this Figure, we compare a novel SRAM cell with conventional SRAM.

Figure 5 (b) shows the write access time for proposed SRAM array under different values of power supply voltage in 130 nm CMOS technology at 298K temperature. The write delay increases significantly when the power supply voltage drops below 0.6V, approximately about two times lower than the previous 6T-SRAM cell in the varies power supply voltage level.

Figure 5 (c) shows the active energy consumption in a BL column during read and writes operation. Consequently, after each read cycle the BL is precharged again to VDD to compensate charge loss. A large number of cells in a bit-line and consequently a large bit-line capacitance will lead to large active energy consumption. In this Figure, A novel SRAM cell with conventional SRAM for 128 and 256 numbers of cells per BL is compared.

3.3. Simulation Results

In this paper, to verify correct operation of proposed SRAM cell and comparison with conventional SRAM cell, proposed SRAM cell is simulated by HSPICE software using 130 nm CMOS TSMC technology. Table.1 shows the simulation results with 1.2V supply voltage. During the two states for Q, a leakage current of new 4T-SRAM cell is lower than conventional SRAM. A new 4T-SRAM has low read and write delay and power consumption.

For testing the correctness of a read and write operation of novel SRAM cell, we write '1' in the new 4T SRAM cell and then read it. Figure 6 shows this

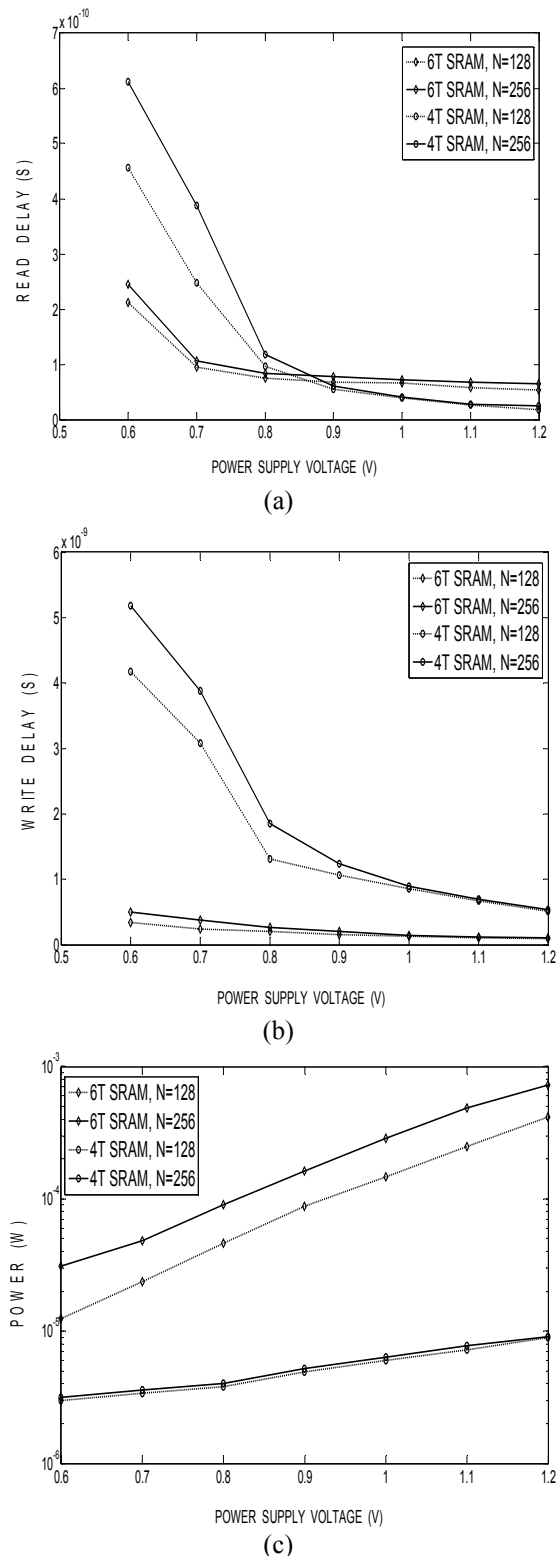


Fig. 5. (a) Read delay. (b) Write delay. (c) Power

correct operation for new 4T-SRAM cell. Following diagrams are the signals shown in the simulation results: “WL” corresponds to the WL signal of row 0 in the

SRAM array. “DT-IN” corresponds to the input data bits; “re” corresponds to the read enable signal given to the sense amplifier circuits; “DT-O” corresponds to the output data bits of the sense amplifier circuits.

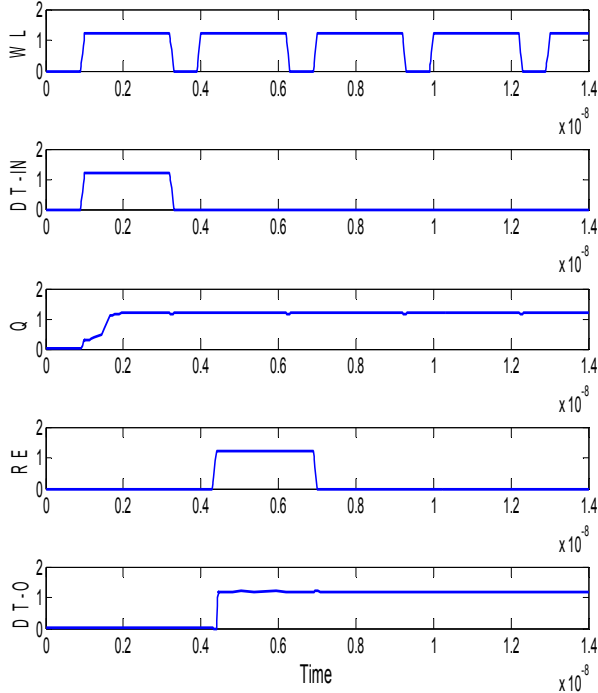
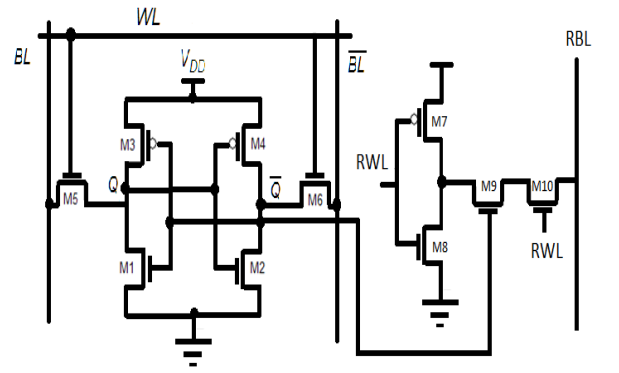


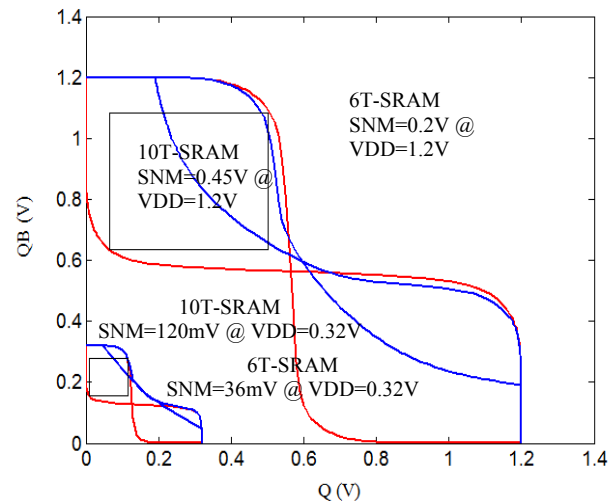
Fig. 6. Operation of a new 4T-SRAM cell

4. A NEW 10T-SRAM CELL

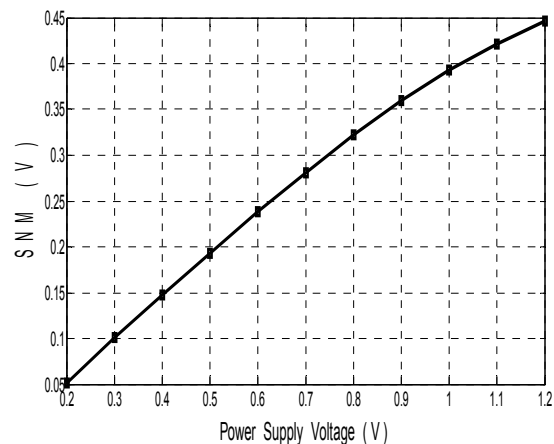
A new 10T SRAM cell structure is shown in Figure 7 (a). In the conventional cell used 6 transistors, but in this structure, 10 transistors is used. The circuit consists of two cross coupled inverters (M1 , M4) and two access transistors (M5 , M6) for write operation is similar to 6T SRAM cells and used four transistors for read operation (M7 , M10). Before the cell is accessed, the read bit-line (RBL) and the write bit-lines (BL, BLB) are precharged to VDD. During the read operation, at the first, RBL precharged to VDD and then RWL asserted to VDD (RWL=1) and then depends on the QB value, RBL discharged through M7, M8 and M9. During the read operation, if the cell is not access, the drain of M10 is asserted to VDD to make the bit-line leakage from this node to RBL. This technique allows a large number of cells to attach RBL. In the same condition, the proposed 10T SRAM cell has higher SNM than conventional 6T SRAM cell. The proposed SRAM has an SNM of 110mV at the supply voltage of 0.32V. Due to having separate read and write operation in the proposed cell, this result is happen. Figure 7 (b) presents the comparison SNM of 6T and 10T SRAM cell. Figure 7 (c) shows variation of SNM versus power supply voltage in the new 10T SRAM cell. In the new structure, the write operation is similar with 6T SRAM cell.



(a)



(b)



(c)

Fig. 7. (a) a new 9T-SRAM cell. (b) SNM curve. (c) Read SNM

4.1. Leakage Current of 10T-SRAM Cell

The leakage current of the proposed 10T SRAM cell when the cell is unaccessed is shown in this part. Figure 8 shows the schematic of bit-line. The number of cells per bit-line depends on leakage current and the leakage current depends on the data stored on the cells.

In the proposed 10T SRAM cell, when the cell is unaccess, the leakage current problem reduced by turning on M10 (RWL = 0). So, the node A voltage is held to VDD and the leakage current increase I_{read} .

Simulation results show the RBL voltage in 512 row cell using HSPICE. As shown in Figure 8, the RBL voltage for data '1' is higher than data '0' and has 200mV bit-line swings for power supply voltage of 0.32V and 512 cells per bit-line.

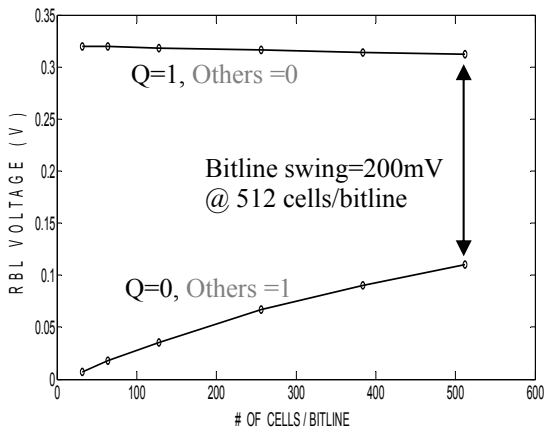
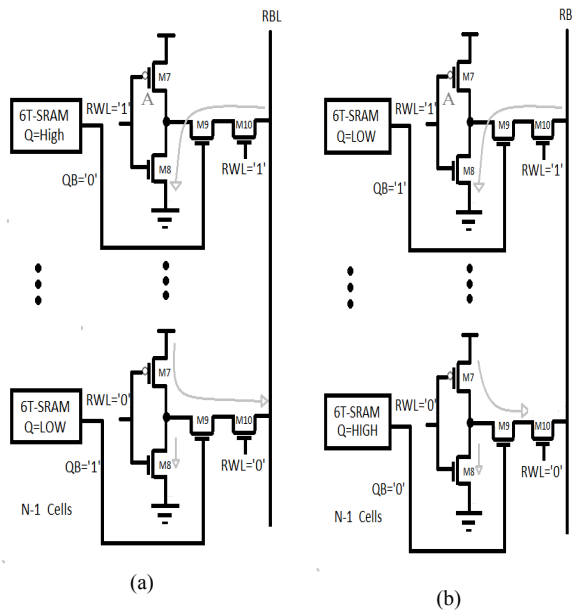


Fig. 8. Leakage current.

4.2. Simulation Results

In this section, we will describe the two performance parameters of memory cell, namely the access time and active energy consumption for proposed 10T SRAM cell. For measuring the write and read access times a 512 rows, 128 columns cell array has been built.

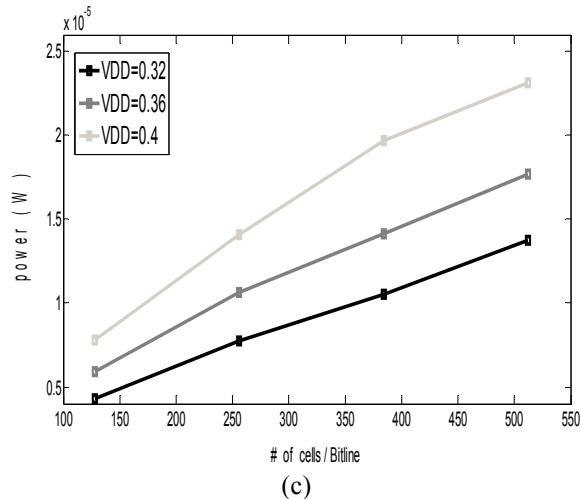
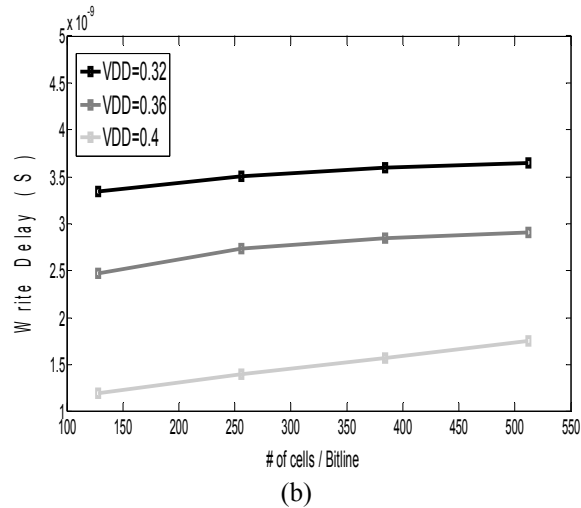
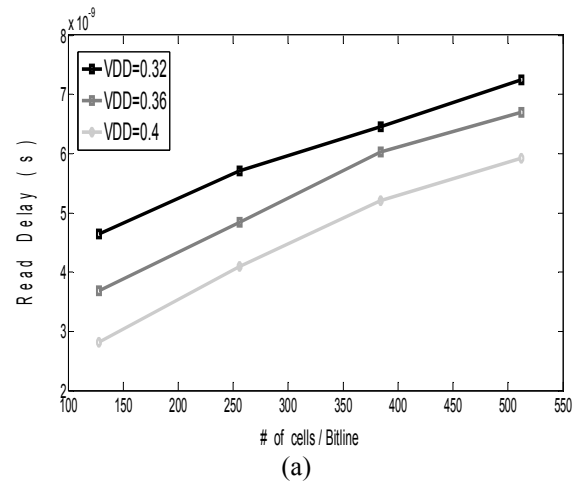


Fig. 9. a) Read delay. (b) Write delay. (c) Power

As shown in Figure 9 (a), a low VDD causes a low read current, results in a high read delay. This Figure showed read access time for this SRAM array under different values of cells per bit-line in 130 nm CMOS technology at 298K temperature. As shown in Figure 9 (a), if the number of cell per RBL is

increasing, resulting in a high Taccess.

Figure 9 (b) shows the write access time for proposed SRAM array under different values number of cells per bit-line in 130 nm CMOS technology at 298K temperature. The write delay increases significantly when the power supply voltage drops.

Figure 9 (c) shows the active energy consumption during read and writes operation. Consequently, after each read cycle the RBL, BLB and BL are precharged again to VDD to compensate charge loss.

A large number of cells in a bit-line and a large bit-line capacitance will lead to large active energy consumption.

5. A NEW 11T-SRAM CELL

A new 11T SRAM cell structure is shown in Figure 10 (a). Write operation is similar to 6T SRAM cells and in the new structure. Five transistors for read operation (M7, M11) are used. Precharge circuit is not used in this structure. Before the cell is accessed only the write bit-lines (BL, BLB) are precharged to VDD. A 10T-SRAM cell is presented in [7], but in the proposed structure, transistor M7 is applied for RBL in order to gets Q data in direct structure , not for use precharge circuit. During the read operation, RWL asserted to VDD (RWL=1) and then depends on the QB value RBL go to high or low level and gets Q value. During the read operations, if the cell is not access, the drain of M10 is asserted to VDD to make the bit-line leakage from this node to RBL. This technique allows a large number of cells to attach to RBL.

In the same condition, the proposed 11T SRAM cell has higher SNM than conventional 6T SRAM cell. The proposed SRAM has an SNM of 98mV at the supply voltage of 0.27V. As same as proposed 10T SRAM cell, new 11T SRAM cell has separate read and write operation. Figure 4 presents the variation of SNM versus power supply voltage and comparison of 6T and 11T SRAM cell. Figure 10 (b) presents the comparison SNM of 6T and 10T SRAM cell. As shown in this Figure, a new SRAM cell has three times bigger SNM than conventional SRAM cell. Figure 7 (c) shows variation of SNM versus power supply voltage in the new 10T SRAM cell.

5.1. Leakage Current of 11T-SRAM Cell

As same as proposed 10T SRAM cell, a new 11T SRAM lead to applying 512 cells per bit-line by reducing leakage current technique. Figure 8 shows the leakage current of the proposed 11T SRAM cell when the cell is unaccessed. In this technique, a leakage current increase read current of read bit-line (RBL).

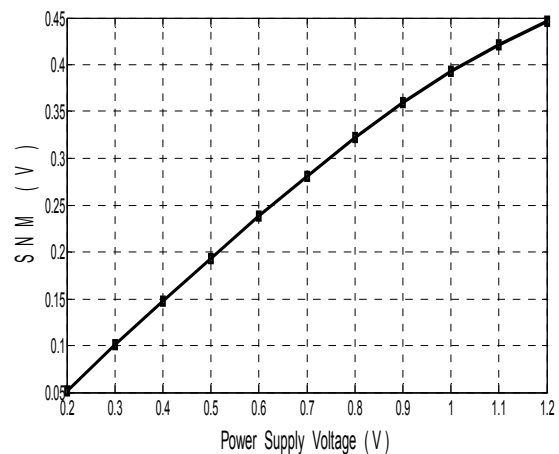
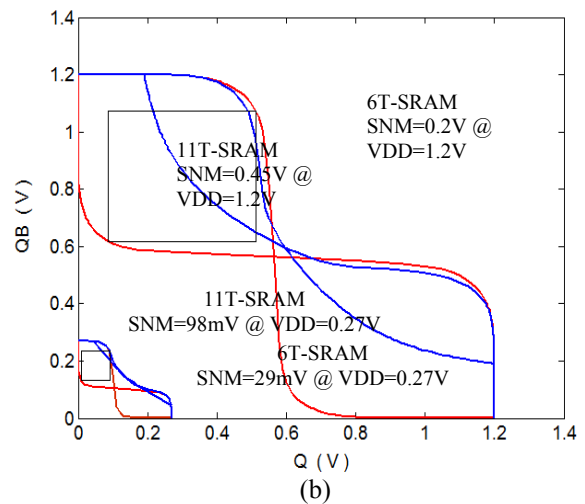
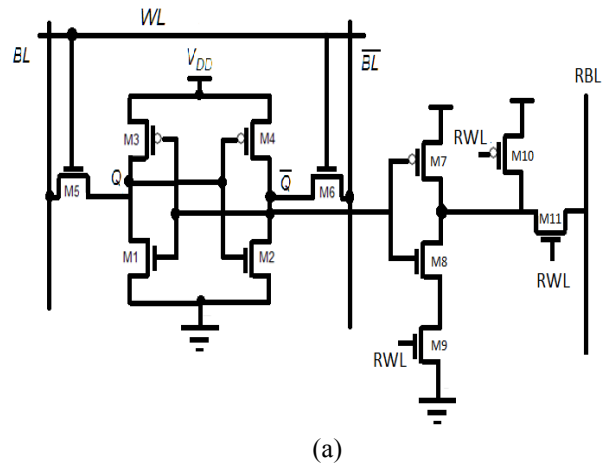


Fig. 10. (a) A new 11T SRAM cell. (b) SNM curve. (c) Read SNM

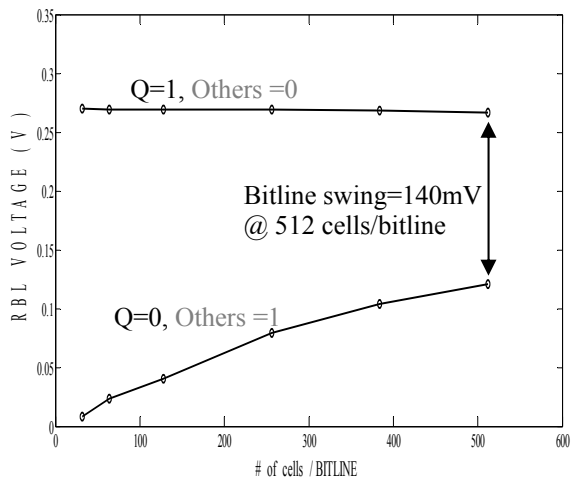
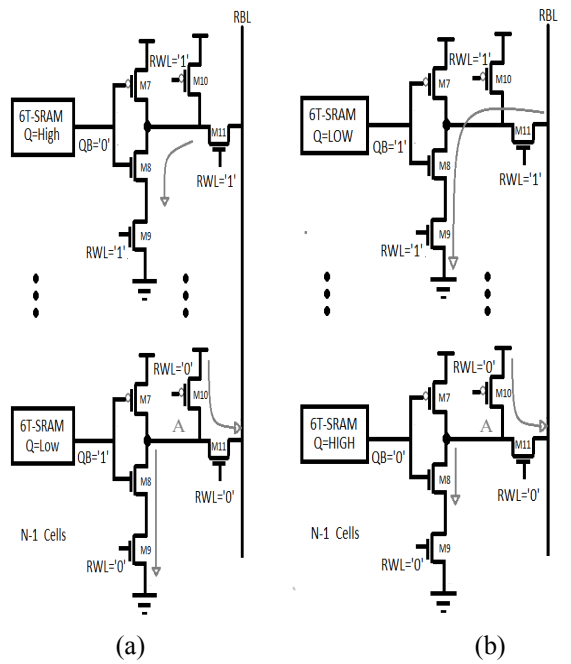


Fig. 11. Leakage current.

In this structure when the cell is unaccessed, the leakage current problem reduced by turning on M10 (RWL = 0). So, the node A voltage is held to VDD and the leakage current make to increase I_{read} .

The maximum cells per bit-line are 512 cells. Figure 8 shows the RBL voltage for data '1' is higher than data '0' and has 140mV bit-line swings for power supply voltage of 0.27V and 512 cells per bit-line.

5.1. Simulation Results

For measuring the write and read access times in this structure, a 512 rows, 128 columns cell array has been built. Simulation results are shown in Figure 12. In 130 nm CMOS technology the 11T SRAM cell achieves the best reads and writes operation at the supply voltage of 0.27V.

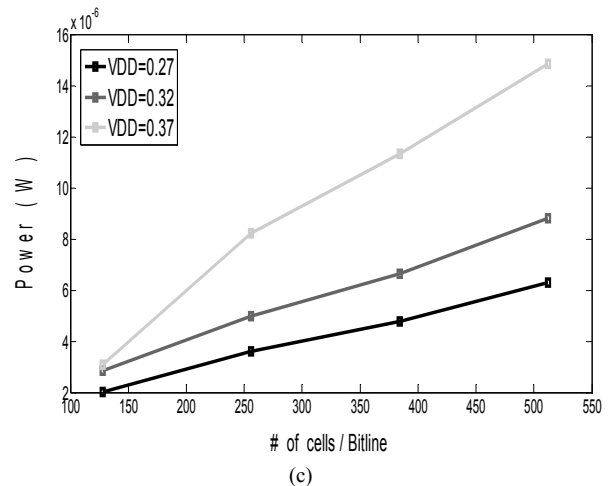
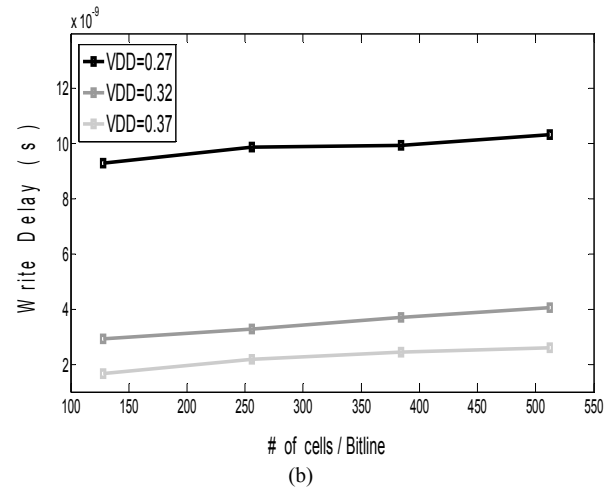
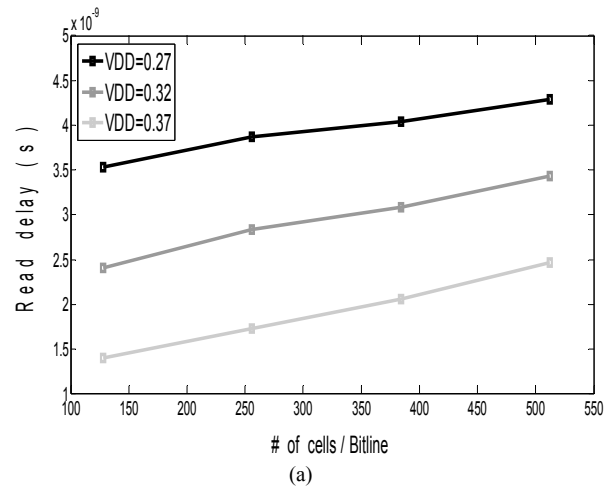


Fig. 12. a) Read delay. (b) Write delay. (c) Power

Table 1 compares these new structures (4T, 10T and 11T) with conventional 6T-SRAM and the other cell proposed in [5], [7] and [10].

6. CONCLUSION

3 new SRAM cells are proposed in this paper. A new 4T SRAM cell has been proposed to accomplish

area and reduce power consumption compared with 6T SRAM cells. Simulation results for 256 cells per bit-line and 128 columns cell array shows that the proposed 4T cell achieves about 18% power saving compared with a 6T cell using 130 nm CMOS technology at power supply voltage of 1.2V.

We proposed a new differential 10T and 11T SRAM cell for the reliable sub-threshold operation. The advantages of these cells are increasing SNM, accomplish area and reduce bit-line leakage problem, thus achieving 512 cells per bit-line. Simulation results show that the proposed 10T cell achieves about 120mV SMN and power of 9.37uW using 130 nm CMOS technology at supply voltage of 0.32V. For new 11T SRAM, SNM is 98mV and power is 6.29uW at supply voltage of 0.27V. In the structure of 11T SRAM cell, precharge circuit is not used. In 130 nm CMOS technology for 512 cells per bit-line and 128 columns cell array, the 10T and 11T SRAM cell achieves the best reads and writes operation at the supply voltage of 0.32V and 0.27V, respectively.

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Table 1. Comparison among our designs and previous SRAM

	6T-SRAM	[5]	[10]	[7]	Proposed 1	Proposed 3	Proposed 4
Technology	130nm	65nm	90nm	130nm	130nm	130nm	130nm
Number of cells on a BL	256	256	256	1024	256	512	512
SRAM cell type	6T	8T	10T	10T	4T	10T	11T
VDD MIN (V)	1.2	0.35	0.3	0.2	1.2	0.32	0.27
POWER (W)	7.259E-4	1.65E-6	3.28E-6	2.04E-6	9.08E-6	9.374E-6	6.299E-6
READ DELAY (S)	6.460E-11	5.48E-9	6.53E-9	3.52E-8	2.442E-11	7.248E-9	4.293E-9
SNM (V)	0.19	0.12	0.1	0.092	0.17	0.12	0.098