A 0.4V, 790µW CMOS Low Noise Amplifier in the Sub-Threshold Region at 1.5GHz

Amin Zafarian[1], Iraj Kalali Fard[2], Abbas Golmakani[3], Jalil Shirazi[4]
1- Department of Electrical Engineering, Islamic Azad University Branch of Arak, Iran
Email: amin_zafarian@ yahoo.ca
2- Institute of Communication Systems and Data Processing, RWTH Aachen University, Germany
Email: iraj.kalali@rwth-aachen.de
3- Department of Electrical Engineering, Sadjad Institute for Higher Education, Mashhad, Iran
Email: golmakani@sadjad.ac.ir
4- Department of Electrical Engineering, Islamic Azad University Branch of Gonabad, Iran
Email: j_shirazi@iau-gonabad.ac.ir

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ABSTRACT:
A fully integrated low-noise amplifier (LNA) with 0.4V supply voltage and ultra-low power consumption at 1.5GHz by folded cascode structure is presented. The proposed LNA is designed in a TSMC 0.18 µm CMOS technology, in which the all transistors are biased in sub-threshold region. Through the use of the proposed circuit for the gain enhancement in this structure and using forward body bias technique, a very high figure of merit is achieved, in comparison to the similar structures. The LNA provides a power gain of 14.7bB with a noise figure of 2.9dB while consuming only 790µW dc power. Also, the impedance matching of the input and output circuit in its operating frequency is desirable and in the whole circuit bandwidth, input and output isolation is below -33dB.

KEYWORDS: Low noise amplifier, Folded cascode structure, Forward body bias, Ultra low power, Ultra low voltage.

1. INTRODUCTION

NCREASING demands for the mobile wireless systems have stimulated the development of the radio frequency integrated circuits (RFICs). The reduction of the power dissipation causes the battery to last longer in these systems. In applications such as the wireless medical telemetry, the low power consumption plays a significant role. In such applications, the portable device should be able to work with ultra- low supply voltage or environment energy such as solar cells. As a result, the power consumption and supply voltage are the two essential parameters which should be optimized by the designer [1]. Considering the fact that LNA is a key part in the RF front-end receivers, designing this stage is full of trade-offs between the input and output impedance matching, the minimum noise figure, the appropriate gain, the high linearity, and the satisfactory isolation between the output and input of the amplifier. Additionally, in portable systems, optimization and developing a balance between the above mentioned parameters would be more complicated, considering power consumption and supply voltage. One of the restrictions of designing LNAs with low power consumption is the threshold voltage (V_t) of the MOSFETs and it has been a serious challenge for the manufacturers of the semiconductor devices to reduce it [2]. So far, some techniques have been offered for reducing the power dissipation and the supply voltage such as biasing transistors in the sub-threshold region and applying forward body bias in order to reduce threshold voltage (V_t) [3]-[5]. Also, using non-stacking structures such as complementary current-reused structure and folded cascode structure would be effective in reducing the supply voltage [6]-[9] but on the other hand, in the sub-threshold biasing state, the gain of the amplifier would decrease and the noise figure would increase. Also, in the non-stacking structures, there is the weak isolation between the input and output. Considering the done research into this subject, little research on LNAs simultaneously with ultra- low supply voltage and ultra-low power has been reported [7]. In this study, it is attempted to present a LNA with 0.4V supply voltage and 790µW power consumption and the high figure of the merit by considering the all aspects of designing LNAs with ultra low supply voltage and ultra low power consumption.

This paper is organized as follows: In Section II, the folded cascode structure is reviewed in brief. In section III, the proposed LNA and the related topics are introduced. In section IV the simulation results are

described and compared to the other reported LNAs. Section V presents the conclusion.

2. LNA WITH FOLDED CASCODE STRUCTURE

The folded cascode structure is one of the conventional structures for designing low noise and low voltage amplifiers (Fig. 1). Transistors M1 and M2 form the first and second stage of this structure, respectively. Inductances L_g and L_s are used for impedance matching of the input, and inductance-capacitance network (L_o and C_o) of the output is employed for impedance matching of the output.

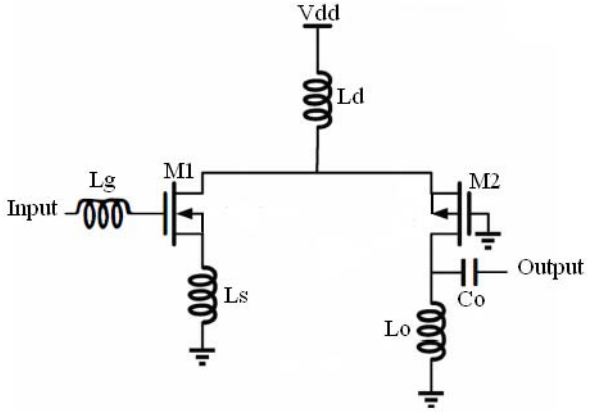

Fig. 1. Schematic circuit of the folded cascode structure

Due to the absence of the stacking gain stages, it is possible to reduce the supply voltage up to the threshold voltage. In addition, it is feasible to slightly reduce the threshold voltage by using forward body bias technique [8,9]. Furthermore, in the folded cascode structure, the parasitic capacitors in drain of the common source transistor (M1) are simply resonated by the inductance L_d at the operating frequency and their effect is obviated/omitted and reduces the noise share of the common gate transistor (M_2) in the output.

One of the shortcomings of the above mentioned amplifier structure is its fairy low gain [8]. Particularly to design amplifiers with extra low supply voltage and power consumption by transistors in the sub-threshold region, transconductance of the transistors decreases dramatically compared to the strong inversion region. The decline in the transistors transconductance on the one hand causes a decrease in gain and on the other hand leads to a rise in the noise figure of the amplifier. The modified structure to overcome the above mentioned problems has been presented in the following section.

3. PROPOSED LNA

Fig. 2 illustrates proposed LNA's schematic circuit.

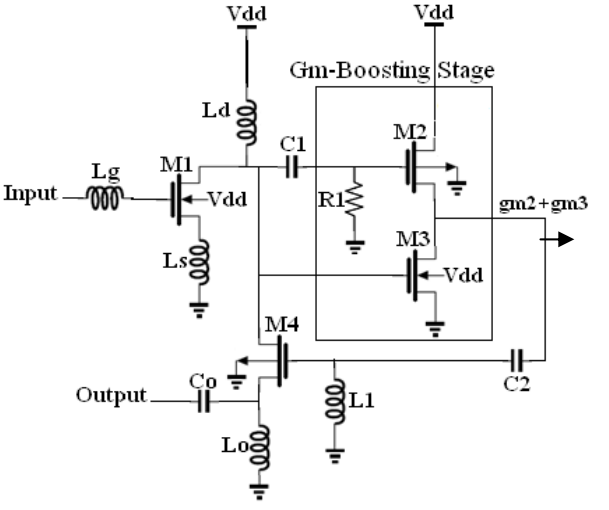

Fig. 2. Schematic circuit of the proposed LNA

In fig (2) the capacitors C_1 and C_2 are coupling capacitors and the resistor R_1 connects the gate of the transistor M_2 to the ground in the DC mode. In order to reduce power consumption, the all transistors are biased in the sub-threshold region. In this region, the current of the MOSFETs' drain (I_d) and their transconductance (g_m) are given by the below equations:

$$I_d = I_0 \exp(\frac{V_{gs}}{\zeta V_t}) \quad (1)$$

$$g_m = \frac{I_0}{\zeta V_t} \exp(\frac{V_{gs}}{\zeta V_t}) \quad (2)$$

Where ζ is the non-ideal factor, V_{gs} is the gate-to-source voltage and V_t is the threshold voltage of the transistor.

Forward body bias technique is employed to reduce supply voltage of the circuit and prevent a substantial drop in the transistors transconductance in the sub-threshold region. Also, to boost amplifier's gain in the sub-threshold region, the circuit shown in square in Fig 2 is added to the folded cascode structure by using G_m-boosting technique [10].

Input signal is amplified by the transistor M_1 and then amplified by added stage including transistors M_1 and M_2 and applied to the gate of the transistor M_4.Thus the gate-to-source voltage of this transistor increases and leads to an increase in its effective transconductance.

As it can be seen from Fig. 2, the transistors M_1 and M_2, added to the folded cascode structure, do not lead to an increase in the supply voltage of the circuit. Also, considering the fact that these two transistors consume the same current and output , the transconductance of this stage is the result of the transconductances of the transistors M_1 and M_2, added together ($g_t=g_{m2}+g_{m3}$). It is possible to lower this stage's current consumption by selecting an appropriate width for these two transistors. Therefore, the proportion of the power consumption to the total transconductance of this stage would be

insignificant in comparison to the common source and common gate stages. In other words, this stage raises the total gain of the circuit with ultra- low power consumption. The power consumption of each stage and transistors' transconductance with 0.4V supply voltage are presented in table 1. The length of the all transistors is 0.18µm.

Table 1. Power consumption of the stages and transconductance of the transistors

	Stage 1 (M_1)	**Stage 2 (M_2 & M_3)**	**Stage 3 (M_4)**
Width (µm)	46×8	64×8 , 22×8	64×8
P_{DC} (µW)	444	176	168
g_m (mA/V)	21	8.5+8.2	8

A. Forward body bias technique

The threshold voltage (V_t) in the MOSFETs is defined as:

$$V_{th} = V_{th0} + \gamma(\sqrt{2\varphi_f - V_{bs}} - \sqrt{2\varphi_f}) \quad (3)$$

Where V_{th0} is the threshold voltage when V_{bs}=0, γ is the body-effect coefficient, φ_f is the bulk fermi potential, V_{bs} is the body-to-source voltage. According to the equation (3), the threshold voltage can be reduced by applying $V_b > V_s$ for n-type transistors and $V_b < V_s$ for p-type transistors.

Fig. 3 demonstrates Simulated threshold voltage (V_{th}), drain current (I_d) and body leakage current (I_{body}) of the MOSFET with a forward body bias for n-type transistor where its width is W=46×8µm and length is L=0.18µm. Applied body biasing voltage is much lower than the turn-on voltage of the P-N junction between the body and source in the MOSFETs (0.7). Thus, the body leakage current could be negligible.

For the p-type transistors with the similar scaling and biasing conditions, by applying V_{body}=0V, the body leakage current and threshold voltage are 2µA and 0.41V, respectively.

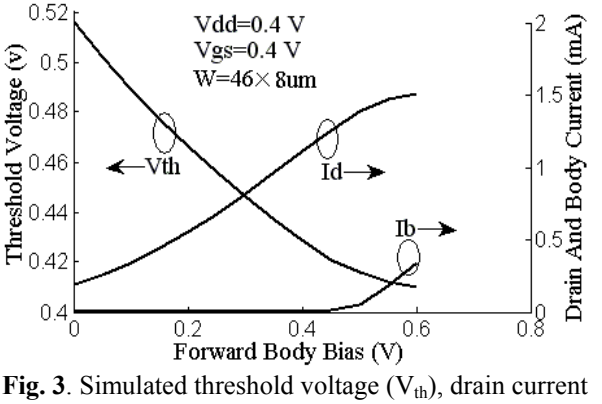

Fig. 3. Simulated threshold voltage (V_{th}), drain current (I_d) and body leakage current (I_{body}) of the MOSFET with a forward body bias sweeping from 0 V to 0.6 V.

B. Circuit analysis

One of the important parameters in designing LNAs is the noise figure which is significantly affected by the input stage. Noise figure in the multistage amplifiers is expressed as follows:

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \ldots + \frac{NF_m - 1}{A_{p1} \ldots A_{p(m-1)}} \quad (4)$$

From equation (4), the added stage to the folded cascode structure causes gain boosting which consequently leads to the noise figure. Due to the use of the inductive degeneration technique, the noise and power matching of the input can be simultaneously achieved. To have a better understanding of the input matching in the first stage, the noise equivalent circuit of the first stage is demonstrated in Fig. 4.

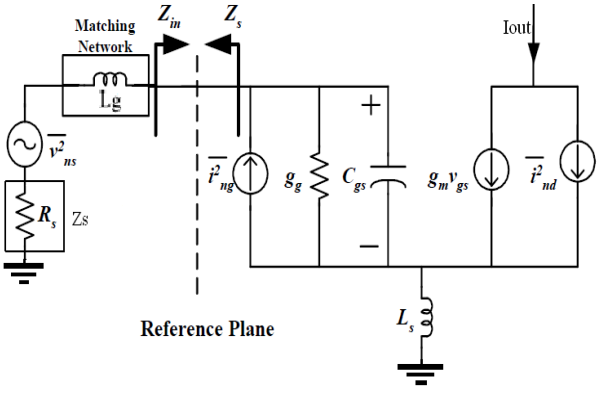

Fig. 4. The small-signal equivalent circuit of the input stage with noise sources

Where $\overline{V_{ns}^2}$ represents the mean-square value of the circuit input noise source, $\overline{i_{ng}^2}$ is the mean-squared value of the induced gate noise current, and $\overline{i_{nd}^2}$ is the mean-squared value of the channel thermal noise current. The expressions of the noise currents in the MOSFETs are given by:

$$\overline{i_{nd}^2} = 4KT\gamma g_{d0}\Delta f \quad (5)$$

$$\overline{i_{ng}^2} = 4KT\delta g_g \Delta f \quad (6)$$

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \quad (7)$$

In the above equations, K is Boltzmann constant, T is the absolute temperature on the Kelvin scale, γ is a constant with a value of 2/3 for long-channel devices, g_{d0} is transistor's transconductance when the drain-to-source voltage (V_{ds}) is zero and Δ_f is the band width. In (6), δ is a constant with a value of 4/3 for long-channel devices. By calculating the total output noise current, $\overline{i_{nout,tot}^2}$,in the small-signal equivalent circuits of the input stage, and divide it by output noise current of the circuit

derived from the input noise source, $\overline{i_{nsout}^2}$, the minimum noise figure of the circuit (F_{min}), noise resistance (R_n)and the optimum source impedance (Z_{opt}) to reach the optimum noise can be derived as follows:

$$R_n = \frac{\gamma}{\alpha g_{m1}} \tag{8}$$

$$F_{\min} = 1 + \frac{2\omega}{\sqrt{5}\omega_T}\sqrt{\gamma\delta(1-C^2)} \tag{9}$$

$$Z_{opt1} = j\left(\frac{1}{\omega C_{gs}} - \omega L_s\right) + \frac{\alpha\sqrt{\frac{\delta(1-|C|^2)}{5\gamma}}}{\omega C_{gs}\left[\frac{\alpha^2\delta(1-|C|^2)}{5\gamma} + (1+\alpha|C|\sqrt{\frac{\delta}{5\gamma}})^2\right]} \tag{10}$$

Where $\alpha=g_{m1}/g_{d0}$ and C are correlation coefficients of the gate noise to the channel noise and equal to 0.395j for long-channel transistors. Based on the small signal analysis, the input impedance of the first stage can be derived as:

$$Z_{in1} = j\left(\omega L_s - \frac{1}{\omega C_{gs}} + \frac{g_m L_s}{C_{gs}}\right) \tag{11}$$

According to (10) and (11), for simultaneous power and noise matching, the following condition should be met:

$$Z^*_{in1} = Z_{opt1} = Z_s \tag{12}$$

By carefully choosing transistor's parameters, it is possible to make real part of the optimum noise impedance equal to the real part of the input impedance in the operating frequency of the circuit.

$$\frac{\alpha\sqrt{\frac{\delta(1-|C|^2)}{5\gamma}}}{\omega_0 C_{gs}\left[\frac{\alpha^2\delta(1-|C|^2)}{5\gamma} + (1+\alpha|C|\sqrt{\frac{\delta}{5\gamma}})^2\right]} = \frac{g_m L_s}{C_{gs}} \tag{13}$$

By employing input matching network (L_g), according to (12), to have maximum power gain and minimum input return loss, the amount of the inductances L_g and L_s at operating frequency of the circuit can be derived from (14) and (15) by choosing proper size for the M_1. Input source impedance (R_s) is assumed to be 50Ω.

$$L_g = \frac{C_{gs} R_s}{g_m} \tag{14}$$

$$(L_g + L_s) C_{gs} \omega_0^2 = 1 \tag{15}$$

In scaling of the transistors M_2 and M_3, the charge carrier mobility in the transistor (μ_x) should be considered. Consider that the electron mobility (μ_n) in the n-type transistors is 2.5 to 3 times more than the whole mobility (μ_p) in the p-type transistors. Therefore, the size of the transistor M_2 should be chosen correspondingly larger than the transistor M_3 size.

4. SIMULATION RESULTS

The proposed LNA has been simulated by HSPICE RF simulator using 0.l8µm CMOS process BSIM3 model. Spiral inductors are used as the inductors and the metal-insulator-metal (MIM) capacitors are used as the capacitors in simulation. Characteristics of the applied devices in the simulation are tabulated in table 2.

Table 2. Characteristics of the applied devices in simulation

Devices	Design Values
M_1	46×8µm/0.18µm
M_2	64×8µm/0.18µm
M_3	22×8µm/0.18µm
M_4	64×8µm/0.18µm
L_s	N=5.5,R=125µm
L_g	N=1,R=35µm
L_d	N=4,R=115µm
L_1	N=2,R=125µm
L_o	N=4.5,R=112µm
C_o	0.6pF

N: Number of the Inductor Turns, R: Inner Radius of the Inductor, For All Inductors W=15µm.

Proposed LNA operates with 0.4V supply voltage and consumes 790µW power. Figures 5 and 6 show the input reflection coefficient (S_{11}) and the output reflection coefficient (S_{22}), respectively. The noise figure of the circuit (NF) and the minimum noise (F_{min}) are shown in Fig. 7. It can be seen from Fig. 7 that the noise figure of the circuit at frequency of 1.5GHz is very close to F_{min} which indicates the desirability of the noise matching of the input. Gain power (S_{21}) and reverse isolation (S_{12}) are depicted in Fig. 8 and Fig. 9, respectively. At1.5GHz, the noise figure and power gain are 2.9dB and 14.7dB, respectively. Also, the input reflection coefficient is -11dB and the output reflection coefficient is less than -20dB. In the whole bandwidth of the circuit, isolation is less than -33dB.

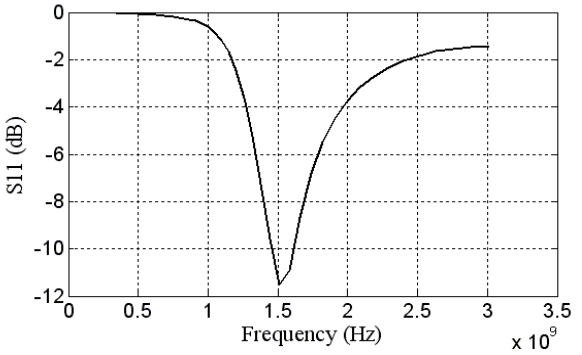

Fig.5. Simulated input reflection coefficient

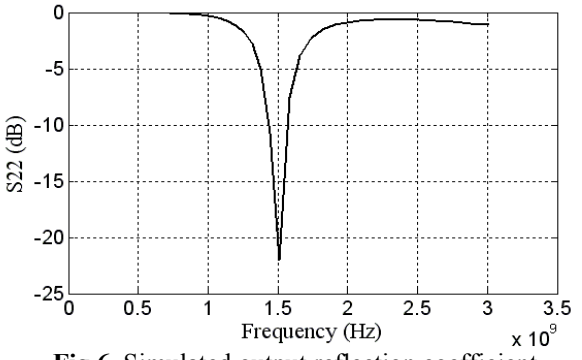

Fig.6. Simulated output reflection coefficient

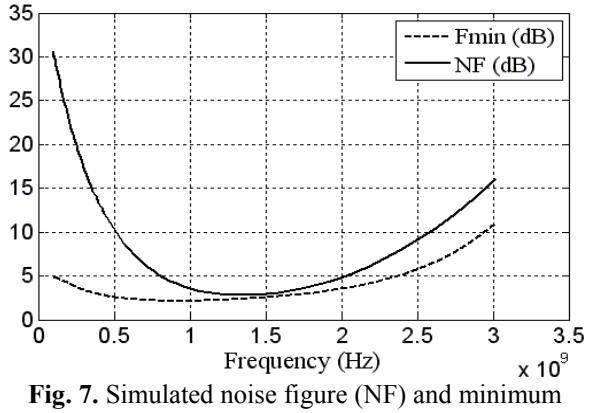

Fig. 7. Simulated noise figure (NF) and minimum noise(F_{min})

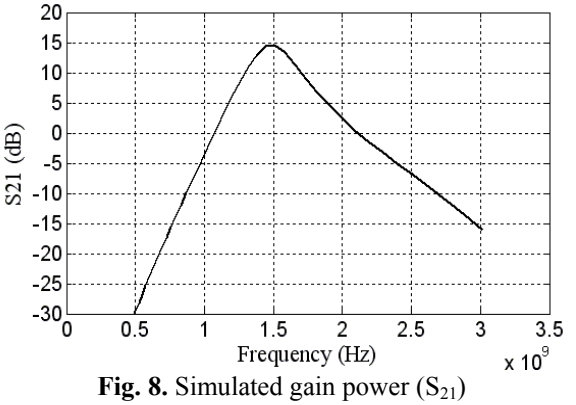

Fig. 8. Simulated gain power (S_{21})

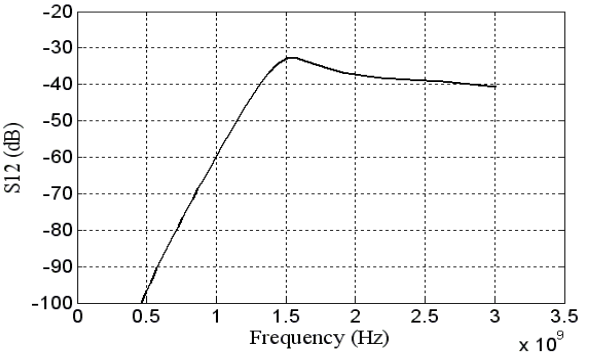

Fig. 9. Simulated reverse isolation (S_{12})

In order to evaluate linearity of the proposed LNA, a two-tone test was conducted. For this purpose, two single-tone signals with identical power at the frequencies of 1.5 GHz and 1.51 GHz were applied to the circuit to measure 1dB compression point and input third order intercept point ,IIP3 (Fig. 10). The 1dB compression point and the input third order intercept point were measured as -11.14dBm and -23 dBm, respectively.

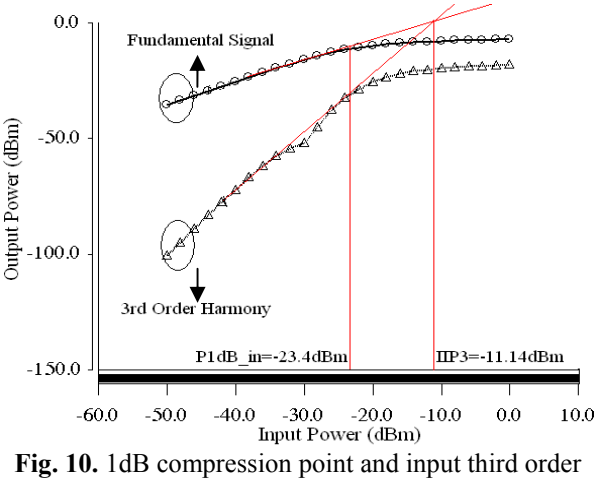

Fig. 10. 1dB compression point and input third order intercept point (IIP_3)

To evaluate the performance of the LNAs and to draw a better comparison between them, the various figures of the merit are defined and used. A commonly used figure of the merit (FOM_1) is the ratio of the power gain to the dc power consumption. Furthermore, it can be extended to include the NF and supply voltage as follows [9]:

$$FOM_2 = \frac{Gain[abs]}{NF[abs]V_{DD}[v].P_{DC}[mW]} \quad (17)$$

FOM_1 and FOM_2 for proposed LNA are 18.6(dB/mW) and 8.81$(V.mW)^{-1}$ respectively. Table III summarizes the performances of the proposed LNA and the data included in the previously published works for comparison.

5. CONCLUSION

In this paper, an ultra- low voltage and ultra- low power LNA in 0.18µm CMOS technology is presented. By adding the proposed circuit for gain boosting (G_m-

boosting stage) of the folded cascode structure and using body bias technique, the performance of the circuit in the sub-threshold region was improved significantly, with only a slight increase in the power consumption. The proposed LNA at 0.4V supply voltage and 0.790µW power consumption has a gain of 14.7dB and noise figure of 2.9dB and at the operating frequency has the desirable input and output impedance matching. Moreover, considering the simulation results, the proposed LNA is perfectly suitable for ultra- low voltage and ultra- low power applications.

REFERENCES

[1] H.-H. Hsieh and L.-H. Lu, **"A CMOS 5-GHz micro-power LNA,"** in *IEEE RFIC Symp. Dig*, pp. 31-34, 2005.

[2] Y. Wang, Z. Khan, K. Iniewski, **"A 0.65V, 1.9mW CMOS Low-Noise Amplifier at 5GHz'',** Proceedings of the 9th International Database Engineering & Application Symposium, IEEE 2005.

[3] H. Lee, S. Mohammadi, **"A 3GHz Subthreshold CMOS Low Noise Amplifier'',** in *proc. IEEE RFIC Symposium*, pp. 494-497, San Francisco, USA, June 2006.

[4] D. Wu, R. Huang, W. Wong, Y. Wang, **"A 0.4-V Low Noise Amplifier Using Forward Body Bias Technology for 5 GHz Application",** *IEEE Microwave and Wireless Companents Letters*, Vol. 17, No. 7, July 2007.

[5] Ch.-P. Chang, J.-H. Chen, Y.-H. Wang, **"A Fully Integrated 5 GHz Low-Voltage LNA Using Forward Body Bias Technology'',** *IEEE Microwave And Wireless Components Letters*, Vol. 19, No. 3, March 2009.

[6] H.-H. Hsieh and L.-H. Lu, **"Design of Ultra-Low-Voltage RF Frontends With Complementary Current- Reused Architectures",** *IEEE Trans. on Microwave Theory and Techniques*, Vol. 55, No. 7, July 2007.

[7] E. Kargaran, M. Mohammad Kazemi, **"Design of 0.5 V, 450 µW CMOS LNA Using Current Reuse and Forward Body Bias Technique",** in *proc. IEEE 5th European Conference on Circuits and Systems for Communications (ECCSC'10)*, Belgrade, Serbia, Nov. 23-25, 2010.

[8] H.-H. Hsieh, J.-H. Wang, L.-H. Lu, "**Gain-Enhancement Techniques for CMOS Folded Cascode LNAs at Low-Voltage Operations'',** *IEEE Transactions On Microwave Theory And Techniques*, Vol. 56, No. 8, August 2008.

[9] E. Kargaran, Gh. Nabovati, M. R. Baghbanmanesh, Kh. Mafmezhad, H. Nabovati, **"An Ultra Low Voltage Ultra High Gain CMOS LNA Using Forward Body Biasing Technique'',** *IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug 2011.

[10] F. Belmas, F. Hameau, J.-M. Fournier, **"A Low Power Inductorless LNA With Double Enhancement in 130 nm CMOS'',** *IEEE Journal Of Solid-State Circuits*, Vol. 47, No. 5, May 2012.

[11] K. Ohsato and T. Yoshimasu, **"Internally Matched, Ultralow DC Power Consumption CMOS Amplifier for L-Band Personal Communications",** *IEEE Microwave and Wireless Companents Letters*, Vol. 14, No. 5, May 2004.

[12] E. Kargaran, H. Kargaran and H. Nabovati, **"A 0.6v Ultra-High-Gain Ultra-Low-Power CMOS LNA at 1.5GHz in 0.18µm Technology",** in *Proceeding IEEE 2nd International Conference on Computer and Electrical Engineering (ICCEE)*, pp. 123-125, Dubai, UAE. December 2009.

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Table 3. Performances summary and comparison of this work and prior published LNAs

Ref.	This Work	[9]	[12]	[5]	[8]	[4]	[3]	[11]
F_0(GHz)	1.5	1.5	1.5	5	5.2	5.1	3	1.6
Technology (µm)	0.18	0.18	0.18	0.18	0.18	0.13	0.13	0.18
V_{DD}(v)	0.4	0.5	0.6	0.6	0.6	0.4	0.6	0.6
Power(mW)	0.79	2.5	2.6	0.8	1.08	1.03	0.4	1.2
NF(dB)	2.9	1.9	2.1	4.1	3.37	5.3	4.7	4.8
S_{21}(dB)	14.7	22	23.1	10.23	10	10.3	9.1	6.4
S_{11}(dB)	-11.5	-9.5	-14	-17.9	-13.4	-17.7	-13	---
S_{22}(dB)	-22	-9.5	-14	-10.6	-10.6	-11.4	-20	---
IIP_3(dBm)	-11.1	-12.5	---	-15	-8.6	---	-11	---
FOM_1	18.60	8.80	8.88	12.79	9.26	10	22.75	5.33
FOM_2	8.81	6.50	5.64	2.63	2.24	2.34	4.02	0.97
Year	2012	2011	2009	2009	2008	2007	2006	2004