Analysis and Design of High Speed 4-2 Compressor in CMOS Technology for High Speed Multipliers

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ABSTRACT:
This review paper contains the discussion about performance analysis of high speed 4-2 compressor architectures, starting from the general idea; conventional form for implementation of this building block along with its truth table has been studied. Thereafter, the modified versions which show promise for high speed multiplier implementations along with their benefits and drawbacks were demonstrated and comprehensively analyzed. Following the same principles, an optimized structure for the 4-2 compressor is obtained which has 2 XOR gate level delay for the critical path and contains the least delay among the reported works. As another advantage, because of uniform paths the output waveforms will be free of any glitches. Simulation results for TSMC 0.18 μm CMOS technology and 1.8V power supply using HSPICE have been provided to show the superiority of our designed architecture in terms of the speed performance. Finally, to confirm the correct behavior of proposed compressor, an 8x8 bit multiplier was designed which can operate at the frequency of 500MHz without employing any special multiplication algorithm for partial product generation.

KEYWORDS: Parallel Multiplier, Booth Encoder, Radix-4, High Speed.

1. INTRODUCTION

In today's electronics, binary multiplier is an inseparable part of commercial applications such as computers, mobile devices and general-purpose microprocessors [1]. Compared to addition and subtraction, multiplication has a more complex process and therefore, its hardware and power consumption is higher [2].

As the definition suggests, in digital electronics the binary multiplier is system utilized for multiplication of two binary numbers. The number which is to be multiplied by the other number is called the multiplicand while the number multiplied is known as multiplier [3]. There are two common methods for multiplication of two binary numbers:

1) The common method which consists of partial product addition and shifting.
2) The algorithmic method which is mainly used in parallel multipliers and employs a certain multiplication algorithm.

It must be noted that although the special purpose multiplication algorithms such as Booth [4], Karatsuba [5], Wallace [6] and Dadda [7] had been introduced in

the 1960s, but until the late 1970s, most of the minicomputers did not contain a multiply instruction, and the procedure of repeatedly shifting and addition of the partial results (Common method) was being utilized [8] which is shown in Fig. 1 for 4-bit multiplication.
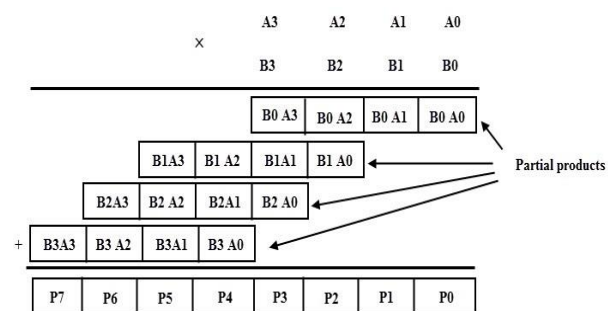

Fig.1. The common method for a 4-bit multiplication.

One of the main obstacles in the hardware implementation of multiplication algorithms was the limitations of VLSI technologies [1, 9]. Recently, the submicron technology improvements have provided the possibility for implementation of the mentioned

multiplication algorithms and so many works have been reported in the literature for hardware realization of parallel multipliers especially Modified Booth Encoded (MBE) multipliers [10-17].

Although in a multiplier the utilization of a multiplication algorithm can significantly boost the speed performance, the most significant part of total delay belongs to the partial product reduction stage mostly consisting of compressors [11, 12, 18]. As a result, delay reduction for the compressors can significantly affect the latency of the whole system.

One of the major speed enhancement procedures in modern digital circuits is the technique of adding numbers with minimal carry propagation and the principal idea is the reduction of three numbers to two by means of a full adder (FA) [2]. The extension of this idea which is shown in Fig. 2, leads to the implementation of the 4-2 compressor which is composed of two cascaded FAs.
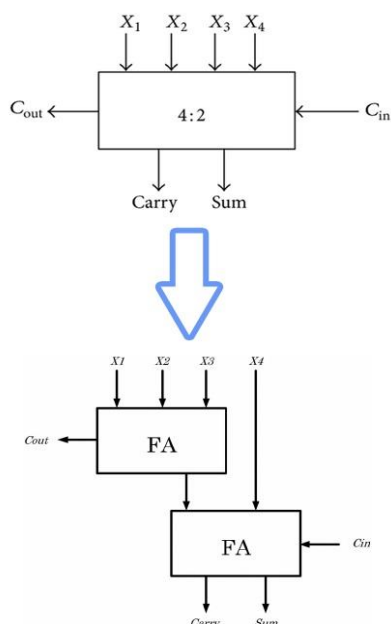

Fig.2. Conventional 4-2 compressor.

According to the conventional structure of Fig. 2, at least a latency of 4 XOR logic gates is expected for implementation of a 4-2 compressor. In recent years so many attempts have been carried out to improve the speed of 4-2 compressors. In [19], Pass Transistor Logic (PTL) is used for speed boosting although it did not result in significant speed performance. In [20], an optimized version has been presented in which the gate level delay was reduced to 3 XOR logic gates. The authors of [21, 22] simplified the conventional truth table for the 4-2 compressor which led to the gate level delays less than 3 XOR gates. In recent years another implementation form based on error tolerant

architectures was employed [23-25] which comprehensively reduced the power dissipation although the gate level delay was not improved and those works were not comparable with structures reported in [20-22] from the viewpoint of speed performance.

In this paper, these architectures were analytically studied and their advantages along with drawbacks have been compared. For better comparison, all their circuits are redesigned and simulated by HSPICE using TSMC 0.18μm CMOS technology and 1.8V power supply. Finally, the optimized 4-2 compressor which has 2 XOR gate level delay is introduced and has been embedded in the body of an 8×8 bit shift/add multiplier in which the measurement of the latency from inputs to the outputs shows that the proposed structure can operate at frequencies up to 500MHz and is suitable for image processing applications.

The organization of the article is as follows. In section 2 the hardware implementation of 4-2 compressor along with high speed architectures are discussed. Section 3 pertains to the optimized architecture for the 4-2 compressor. In section 4 the simulation and comparison of selected architectures along with proposed circuit have been presented while the design explanation of 8×8 bit multiplier is discussed in section 5. Finally, the conclusions have been summarized in section 6.

2. THE 4-2 COMPRESSOR

In 1981 a new structure based on carry save adders has been introduced by Weinberger of IBM [26] in which by means of a horizontal path defined as C_{out}, in addition of two vertical paths (Sum and $Carry$), the interconnection of adjacent cells could be changed in the accumulation stage [18]. This architecture which became famous as the 4-2 compressor is now widely employed in high performance parallel systems to improve the speed of arithmetic operations [22].

As shown in Fig. 2, a 4-2 compressor is a 5-bit adder in which the relation between inputs and outputs can be described as:

$$X_1 + X_2 + X_3 + X_4 + C_{in} = Sum + 2 \times (Carry + C_{out}) \qquad (1)$$

As equation (1) suggests, Carry and C_{out} have equal weighting and have a higher binary bit value in comparison with other bits [22]. Based on this relation, general truth table for implementation of the 4-2 compressor can be as illustrated by Table 1 in which n represents the number of inputs in high logic level.

The simplest structure for implementation of the 4-2 compressor can be obtained by cascading of two FAs which is illustrated in Fig. 2. As completely discussed in [20], at least a latency of 4 XOR logic gates is expected for design of the 4-2 compressor.

In [19], PTL version of the conventional 4-2 compressor has been introduced which is shown in Fig. 3. By defining the latency of XOR/XNOR gates as the normalized unit for gate level delay calculation, it is clear that the delay of NAND/NOR gates will be equal to 0.7 while the corresponding value for inverter will be 0.5.

Table 1. The general truth table of the 4-2 compressor.

n	C_{in}	C_{out}	Carry	Sum
0	0	0	0	0
1	0	0	0	1
2	0	-	-	0
3	0	1	0	1
4	0	1	1	0
0	1	0	0	1
1	1	0	1	0
2	1	-	-	1
3	1	1	1	0
4	1	1	1	1

As a result, the gate level delay for critical path of circuitry in Fig. 3 will be approximately 4 XOR logic gates.
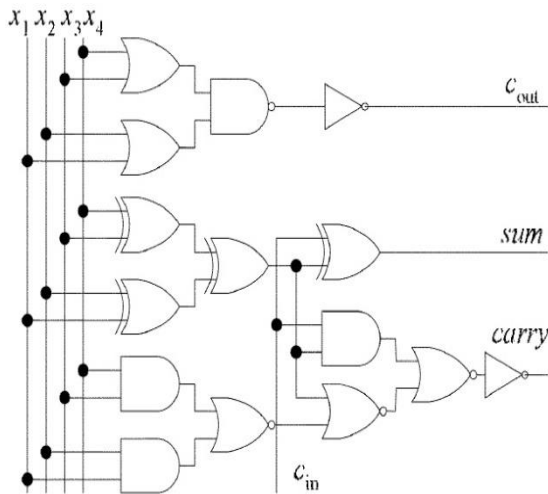

Fig.3. 4-2 compressor designed in [19].

If static logic is used to design this architecture, the total transistor count will be 64 which is fair for implementation of this structure. However, the speed performance would not be interesting which considerably degrades the use of this circuit.

In [20], by means of high speed two output XOR/XNOR gates shown in Fig. 4 and also, by means of structural modification, a novel architecture was introduced for the 4-2 compressor.

The designed architecture which is illustrated in

Fig. 5 is only composed of 6 gates and its transistor count is 60. Also, the gate level delay of 3 XOR logic gates was achieved as an incredible speed enhancement in 4-2 compressor design criteria.

It must be mentioned that this architecture is still employed in body structure of the parallel multiplier design because of its low power consumption feature [27].
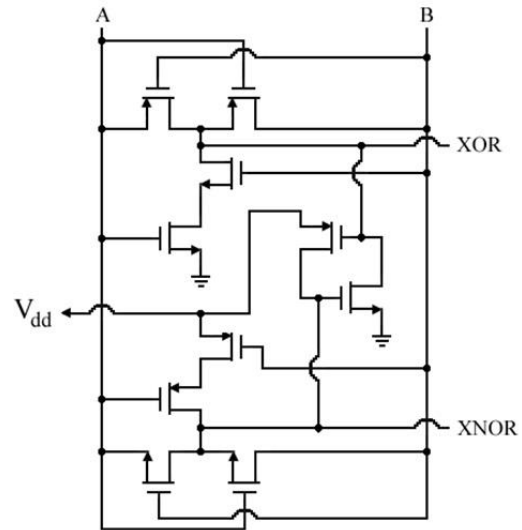

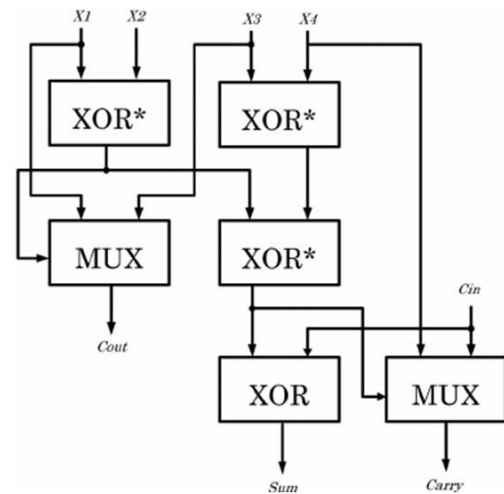**Fig.4.** Two output XOR-XNOR gate proposed in [20].

Fig.5. 4-2 compressor designed in [20].

In 2012, by means of modifications in general truth table described in Table 1, two high speed circuits were introduced for hardware implementation of 4-2 compressors.

If the general truth table is studied carefully, it can be concluded that there are some neutral states for C_{out} and Carry outputs. In [21], this fact is used to divide the truth table to eight different states as shown in Fig. 6.

$C_{in}=0$

n*	C_{out}	Carry	Sum		C_{out}	Carry	Sum	
0	0	0	0		0	0	1	
1	0	0	1		1	0	0	
2	1	0	0		1	0	1	
0	0	0	1		0	1	0	
1	1	0	0		1	0	1	
2	1	0	1		1	1	0	

$I_3=0$ $I_4=0$ (left), $I_3=0$ $I_4=1$ (right); $I_3=1$ $I_4=0$ (left), $I_3=1$ $I_4=1$ (right)

$C_{in}=1$

n*	C_{out}	Carry	Sum		C_{out}	Carry	Sum	
0	0	0	1		0	1	0	
1	0	1	0		1	0	1	
2	1	0	1		1	1	0	
0	0	1	0		0	1	1	
1	1	0	1		1	1	0	
2	1	1	0		1	1	1	

$I_3=0$ $I_4=0$ (left), $I_3=0$ $I_4=1$ (right); $I_3=1$ $I_4=0$ (left), $I_3=1$ $I_4=1$ (right)

• n is number of I_1 and I_2 inputs in which they are equal to logic 1.

Fig.6. Employed truth table for the 4-2 compressor in [21].

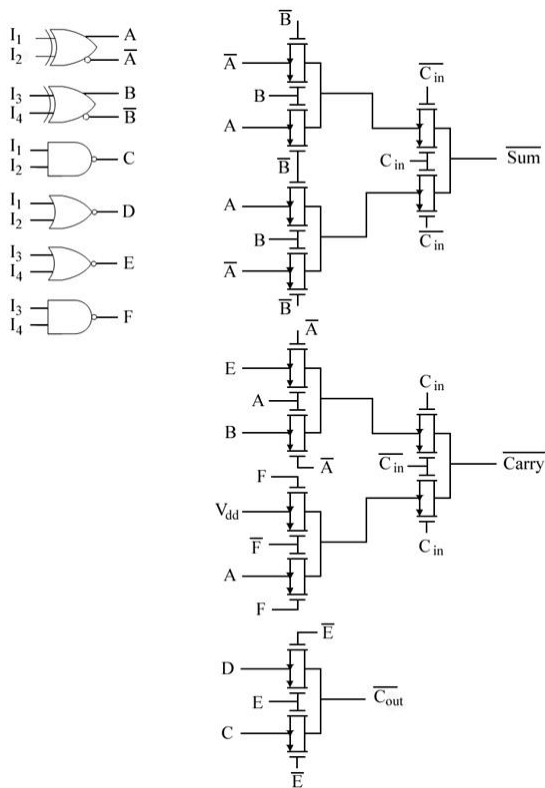Based on this truth table, a new architecture was designed which is shown in Fig. 7.

Fig.7. 4-2 compressor designed in [21].

The authors have claimed that the gate level delay for this structure is about 2 XOR logic gates. But as Fig. 7 depicts, all outputs are in a complementary state which necessitates the use of an inverter gate after each output. Hence, the actual gate level delay will be 2.5 XOR logic gates. But in comparison with [20], the speed performance has been improved. From the power consumption aspect, because of more gate usage for 4-2 compressor implementation of Fig. 7, the structure of Fig. 5 will be more power efficient. Also, the total transistor count for the structure of Fig. 7 is 68 which illustrates another drawback of this circuit in comparison with 4-2 compressor reported in [20].

Considering the same hypothesis utilized in [21], another circuit is reported in [22] in which the gate level delay is reduced to 2 XOR logic gates plus one transistor which is the lowest latency reported in the literature. Fig. 8 shows the corresponding circuitry in which the total transistor count is 70.
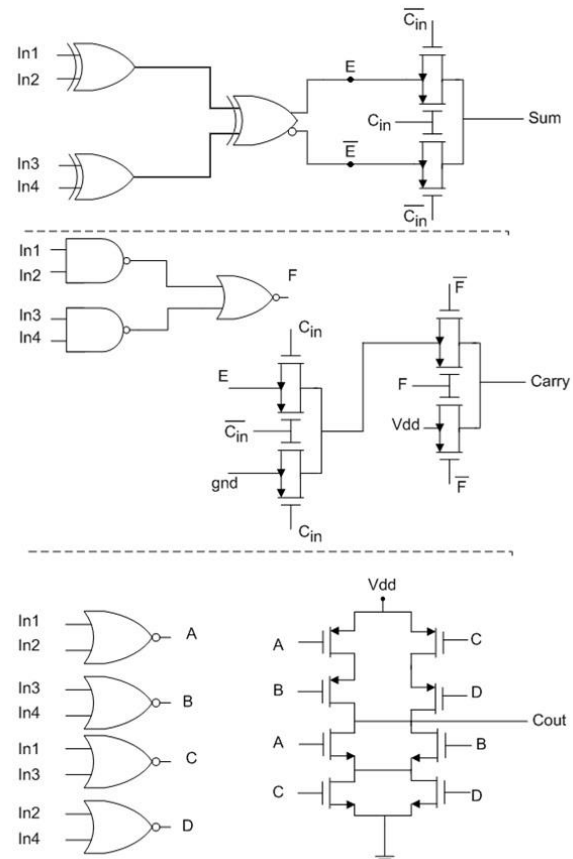

Fig.8. 4-2 compressor reported in [22].

Although the transistor count is higher compared to other works, as the structure is a combination of static logic and PTL, its power consumption is less than [21].

3. THE PROPOSED 4-2 COMPRESSOR

Considering the proposed truth table in Fig. 6, it becomes clear that the outputs of the compressor can be simplified more to achieve fewer latencies compared to the previous architectures. For Sum output we have:

$$Sum = I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus C_{in} \qquad (2)$$

Which is same as previously reported works. The $Carry$ output abides by:

$$Carry = \left[((I_1 \oplus I_2) + (I_3 + I_4)).\,(\overline{(I_1 \oplus I_2)} + \overline{(I_3 + I_4)}) + \overline{C_{in}}\right].\left[\left((I_3.I_4).\left(\overline{(I_3.I_4)} + \overline{(I_1 \oplus I_2)}\right)\right) + C_{in}\right] \quad (3)$$

And, C_{out} can be obtained using:

$$\overline{C_{out}} = \left[\overline{(I_3 + I_4)} + (I_1 + I_2)\right].\left[(I_3 + I_4)(I_1.I_2)\right] \qquad (4)$$

Therefore, by means of employing the truth table of Fig. 6, a novel 4-2 compressor with lower delay can be designed. In the proposed architecture which is shown in Fig. 9, the gate level delay form inputs to the outputs is reduced to 2 XOR logic gates.
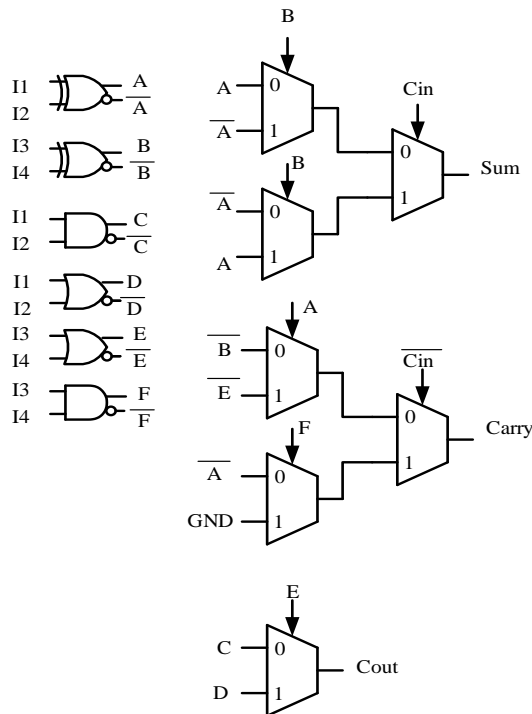

Fig.9. The proposed 4-2 compressor.

The XOR/XNOR gates of Fig. 4 can be used for implementation of the proposed compressor. But in order to reduce the transistor count, the non-full swing XOR and XNOR gates of Fig. 10 which were previously introduced in [22] were employed. The other state is generated by means of an inverter at the end of the corresponding gate and because these double output gates are feeding the multiplexers, their gate level delay will be the same as a normal XOR one.
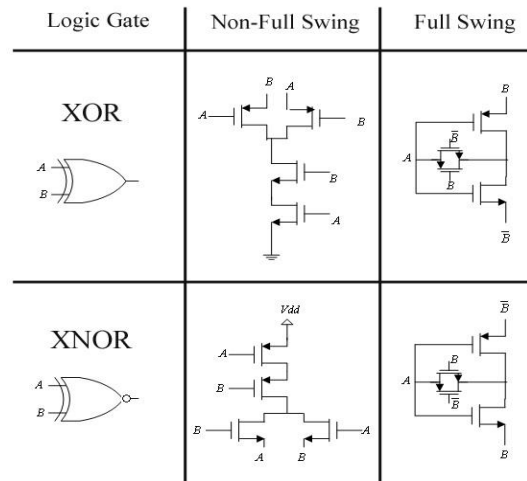

Fig.10. The reported XOR and XNOR gates in [22] used for the proposed 4-2 compressor.

Also, the multiplexers were obtained from the circuits reported in [20] to enhance the speed performance. As C_{in} is generated before than the inputs of the corresponding multiplexer gate, it would not affect the speed performance of the whole structure.

By means of the mentioned gates the transistor count for the designed circuit is reduced to 66 and because there is no need for inverters at the output nodes, the power consumption will be less than the architecture reported in [21].

Also, as the outputs will be fed to another compressor in a multiplier array, the output multiplexers would not degrade the speed performance for the case of compressor cascading.

In addition, the carry rippling feature is the same as structure reported in [21].

4. SIMULATION RESULTS AND COMPARISON

For better comparison between proposed 4-2 compressor and the works discussed in the previous section, simulations using HSPICE for TSMC standard 0.18μm CMOS technology and 1.8V power supply were performed to measure the delay and power consumption of our work and redesigned architectures reported in [19], [20], [21] and [22]. In order to provide a realistic simulation environment, each circuit is loaded with buffers.

The propagation delay was measured from the point where the earliest transition reaches 50% of V_{dd}, to 50% V_{dd} of the latest output signal [20]. Fig. 11 shows the simulation result for propagation delay of the proposed 4-2 compressor which is equal to 854ps.
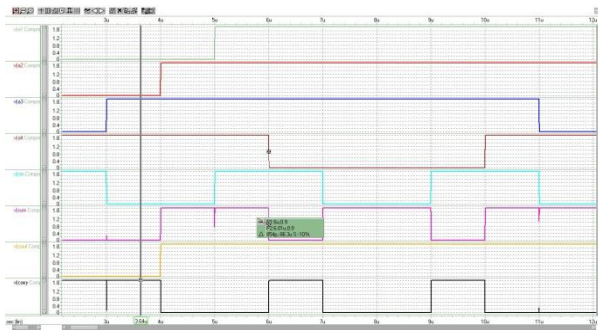
Fig.11. Simulation result for delay measurement of the proposed 4-2 compressor.

Also, the comparison result for delay measurement which is shown in Fig. 12, demonstrates that the lowest value of delay belongs to our circuit. The second best work is the structure of [21] as we do not consider the inverters after the outputs.
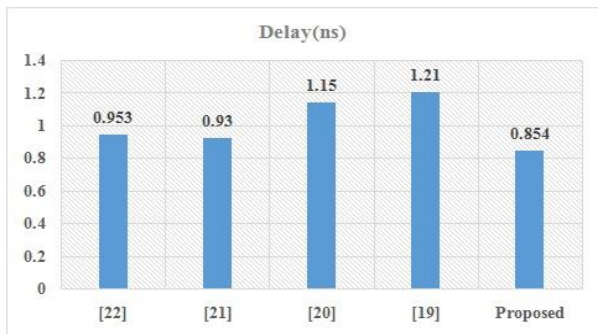

Fig.12. Delay comparison between our work and redesigned 4-2 compressors simulated with TSMC 0.18μm CMOS technology.

Finally, the measurement result for power dissipation which is shown in Fig. 13, demonstrates that the lowest value of power consumption belongs to [20], while our proposed circuit captures the second place. It must be mentioned that the power dissipation for all works is measured at the operating frequency of 1MHz.
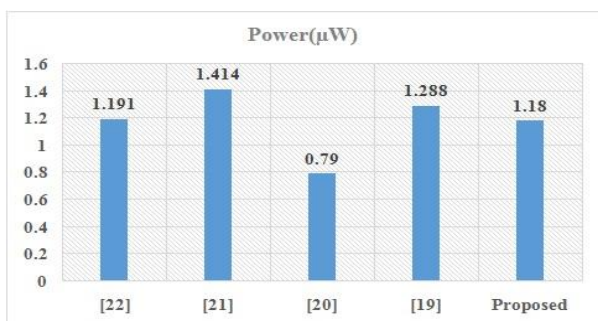

Fig.13. Power dissipation comparison between our work and redesigned 4-2 compressors simulated with TSMC 0.18μm CMOS technology.

Also, Table 2 illustrates the comparison between these works based on their circuitry and simulation results obtained by the authors.

Table 2. Comparison between selected MBE architectures.

Work	Proposed	[19]	[20]	[21]	[22]
Technology (μm)	0.18	0.18	0.18	0.18	0.18
Transistor Count	66	64	60	68	70
Gate Level Delay (XOR)	2 gates	4 gates	3 gates	2.5 gates	2.25 gates
Power (μm) @1MHz	1.18	1.288	0.79	1.414	1.191
Delay(ps)	854	1210	1150	930	953

It must be mentioned that there are other states of the art works reported in the literature which have not been considered in this article as they were not comparable from the viewpoint of speed performance.

5. THE MULTIPLIER DESIGN

In order to evaluate the performance of the designed compressor, an 8x8 bit shift and add multiplier has been implemented. The architecture of designed multiplier is shown in Fig. 14.
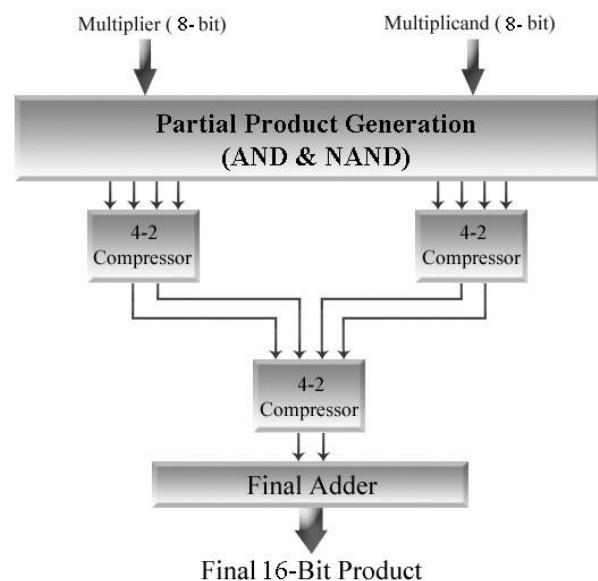

Fig.14. The structure of designed multiplier.

The final stage for addition is also implemented by FAs. Based on simulations by HSPICE for TSMC standard 0.18μm CMOS technology and 1.8V power supply, the measured delay for designed 4-2

compressor was 260ps, while the obtained latency for 16 Bit addition was 1300ps.

As a result, the total measured latency of the system, considering partial product generation, partial product reduction and final summation was 1920ps, which guarantees the operation of the designed multiplier at the frequencies up to 500MHz. Table 3 illustrates the design specifications of the proposed multiplier.

Table 3. Design specifications of the proposed multiplier.

Technology(μm)	0.18
Power Supply(V)	1.8
Propagation Delay(ps)	1920
Operating Frequency(MHz)	520

6. CONCLUSION

In this paper the performance of high speed 4-2 compressor design has been reviewed literally and a new high-speed architecture has been introduced which can be widely employed in high frequency multiplier design. All benefits along with the drawbacks of the best reported works were studied carefully to provide a better analytical view for the reader.

Compared to previous works, a 12% speed improvement has been achieved in which the simulation results confirm the correctness of design considerations. Also, from the viewpoint of power consumption, the designed circuit shows good behavior as the need for output inverters has been eliminated.

Simulation results by HSPICE for the proposed circuit using TSMC standard 0.18μm CMOS technology and 1.8V power supply show a delay of 854ps for the high capacitive load while the measured delay for the case of unit inverter based load is 260ps which demonstrate the superiority of implemented circuit over previous designs. Also, the designed multiplier which can be widely used for image processing applications can operate at the frequency of 500MHz.

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