A New Low Power, Area Efficient 4-bit Carry Look Ahead Adder in CNFET Technology

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Received: June 2021 Revised: August 2021 Accepted: October 2021

ABSTRACT:
In this paper, a new hybrid low-power and area efficient Carry Look-Ahead Adder in CNFET technology based on the full-swing Gate Diffusion Input (GDI) technique is proposed. The proposed CLA design in GDI logic style, not only decreases the circuit area effectively but also decreases the power consumption and delay parameters as well. The proposed design is simulated in HSPICE using the CNFET model parameters. Finally, the simulation results justify a good improvement in the circuit performance parameters such as power consumption, delay, chip size area and power-delay product (PDP) for the proposed CLA circuit.

KEYWORDS: Low-Power, Area-efficient, Carry Look-Ahead Adder, GDI, CNFET.

1. INTRODUCTION

Power consumption and area reduction of digital logic and memory circuits have been the primary priorities of the digital integrated circuit designers which drew their most attention in the design of digital integrated circuits[1]. Scaling-down the chip size area could be possible by decreasing the number of transistors as well as reducing the size of the transistors[2]. Meanwhile, decreasing the number of transistors to implement a circuit design, leads to a positive effect in reducing the chip size area [3]. Moreover, shrinking down the silicon transistors like MOSFETs, leads to many higher-order problems such as high leakage currents, effects of short transistor channel lengths and etc. [4]. To overcome the abovementioned problems, some emerging technologies are presented in the previously published literature, such as: Quantum Cellular Automata (QCA) [5]–[8], Single Electron Transistor (SET) [9] and Carbon Nano-Tube Field Effect Transistor (CNFET))[10]–[12]. However, among the mentioned emerging technologies, CNFETs are considered as a suitable alternative for CMOS transistors because they show a very close circuit behavior to the CMOS technology[13]. Moreover, CNFET technology benefits from having unique Characteristics such as lower power consumption, lower parasitic capacitances and higher power-delay efficiency in comparison with the conventional CMOS technology[14], [15]. A CNFET device consists of single walled CNT (SWCNT) as the conducting channel, which can operate as either conductor or a semiconductor depending on the angle of atom arrangement pattern along the tube, which is called as "chirality vector" (n, m) [16].

Furthermore, the threshold voltage of a CNFET depends to the diameter of CNT, can be calculated by Eq. (1).

$$V_{th} \approx \frac{E_g}{2e} \approx \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \quad (1)$$

Where, a= 2.49Aº is the (carbon to carbon) atom distance and Vπ= 3.033 eV is the carbon π-π bond energy in tight bonding model. Moreover, (e) is the charge of an electron and D is the diameter of a nanotube. Furthermore, the diameter of a nanotube can be computed using Eq. (2):

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \quad (2)$$

Where, a_0 = 0.142nm, is the inter-atomic distance between the centers of two adjacent Carbon atoms.

On the other hand, "Full-Adder" is one of the most basic functional parts of a processor as well as a computational system, so, employing a high speed and

Paper type: Research paper
DOI: https://doi.org/10.52547/mjee.16.1.65
How to cite this paper: A. Ghorbani, M. Dolatshahi, S. M. A. Zanjani and B. Barekatain, **"A New Low Power, Area Efficient 4-bit Carry Look Ahead Adder in CNFET Technology"**, *Majlesi Journal of Electrical Engineering*, Vol. 16, No. 1, pp. 65-73, 2022.

low power full-adder can significantly improve the computational efficiency and overhead of other related operations such as multiplication, division, subtraction and etc.[17]. Therefore, in order to reduce the power consumption of the abovementioned operations, adders should be designed in a reduced chip area by having fewer transistors. Many design techniques have been proposed to improve the power consumption and area as well as the overall performance of digital circuits [18]–[20].

Moreover, the carry look ahead adder (CLA) [21] is a type of the parallel multi-bit adder which significantly reduces the delay of the carry propagation by using a design methodology that defines carry-propagate and carry-generate terms as the main design parameters and signals. Generally, in conventional carry ripple adder structure, each adder block waits for the carry which is generated by its previous block. So, such a circuit latency (delay) increases significantly. However, the carry look ahead adder [22] implements based on the Carry-generate (G) and Carry-propagate (P) signals which are expressed by the equations that are given in Table. 1.

Table 1. Carry-generate (G) and Carry-propagate (P) functions in the CLA.

$P_i = A_i \oplus B_i$ $G_i = A_i \cdot B_i$
$C_0 = INPUT$ $C_1 = G_0+P_0.C_0$ $C_2 = G_1+P_1.C_1=G_1+P_1.G_0+P_1.P_0.C_0$ $C_3 = G_2+P_2.G_1+P_2.P_1.G_0+P_2.P_1.P_0.C_0$ C_4 $=G_3+P_3.G_2+P_3.P_2.G_1+P_3.P_2.P_1.G_0+P_3.P_2.P_1.P_0.C_0$
$S_0 = C_0 \oplus P_0$ $S_1 = C_1 \oplus P_1$ $S_2 = C_2 \oplus P_2$ $S_3 = C_3 \oplus P_3$
$P_0 = A_0 \oplus B_0$ $P_1 = A_1 \oplus B_1$ $P_2 = A_2 \oplus B_2$ $P_3 = A_3 \oplus B_3$
$G_0 = A_0.B_0$ $G_1 = A_1.B_1$ $G_2 = A_2.B_2$ $G_3 = A_3.B_3$

Where, C_i is the carry generated by the i_{th} stage and S_i is the Sum output resulted from the i_{th} stage, and A, B are the inputs.

Furthermore, the Gate Diffusion Input (GDI) technique is one of the solutions that successfully is used as a low-power technique which benefits from the low transistor count and circuit complexity [20], [21], [23].

So, the main contribution of this paper is to improve the performance of a 4-bit carry look ahead adder employing the GDI technique. The proposed CLA benefits from the full swing GDI gates which has properly reduced the number of transistors and also decreased the power consumption. So, the rest of this paper is organized as follows: the GDI technique is introduced in Sec. 2. The previously published adders are discussed in Sec. 3. Moreover, the new 4-bit CLA in CNFET technology is proposed in Sec. 4. While the simulation results and comparison of the proposed 4-bit carry look ahead adder cell with other designs are presented in Sec. 5. Finally, some conclusions are presented in Sec. 6.

2. GDI TECHNIQUE

The basic GDI cell is very similar to a conventional inverter circuit that is shown in Fig. 1, except that the sources of N and P type transistors are connected to the inputs of "P" and "N" instead of ground (GND) or supply voltage (VDD) [20]. In other words, the "P" and "N" nodes operate as external inputs in the GDI cell. Therefore, different logical functions can be implemented using this structure, which are summarized in Table. 2 [20].

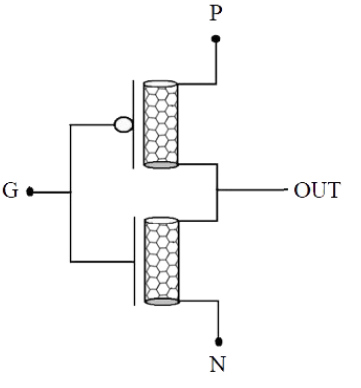


Fig. 1. Basic structure of GDI gate using CNFETs[20].

Table 2. Different logical functions which can be implemented using GDI cell [20].

N	P	G	OUT	Function
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}$B+AC	MUX
'0'	'1'	A	$\bar{A}$	NOT

However, the number of transistors is properly reduced by using the GDI technique, but, the main problem of this method is that the output signals are not full-swing. The full-swing GDI gates are presented in [20], [24] to solve this problem. Generally, the main contribution of [20], [24] was providing full-swing outputs for the both logic "1" and logic "0" by using swing Complementary transistors.

3. THE PROPOSED DESIGN

As it is shown in Fig. 2, the Carry Look Ahead Adder structure consists of 3 major stages.

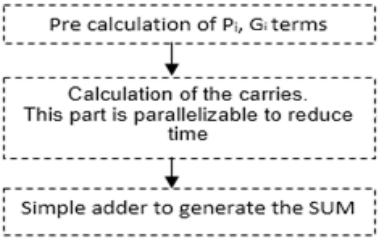


Fig. 2. The 3-stage structure of the CLA adder.

In this paper a new CLA is simulated and implemented by combining the GDI logic style with the CLA logical equations summarized in Table. 1. In the proposed CLA circuit, the carry propagation delay is decreased due to the fact that all the signals are produced in a semi-parallel manner and at the same time it is not necessary to wait further for the previous stages' result. The Gi and Pi circuit structures which are used in the proposed design are shown in Fig. 3 and implemented with 3 and 4 transistors, respectively [20], [24] . However, these structures are designed based on the GDI technique and also have full-swing outputs. Furthermore, the proposed CLA design is implemented using the GDI logic style shown in Fig. 4.

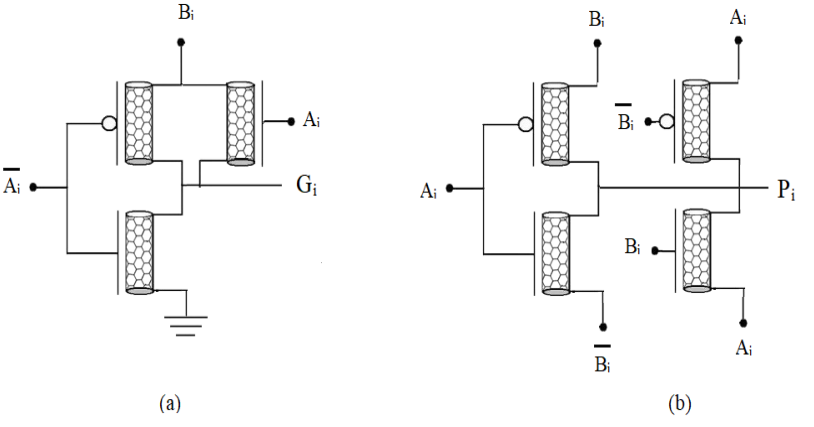


Fig. 3. The full-swing GDI gates: (a) AND for Gi and (b) XOR for Pi.

As it is shown in Fig. 3a, the carry-generate (Gi) logical function is designed with 3 transistors as a full-swing GDI "AND" gate. Moreover, the carry-propagate (Pi) logical function is designed with 4 transistors as a full-swing GDI "XOR" gate that is shown in Fig. 3b. Furthermore, as shown in [25], the XOR and AND gates are designed with 12 and 6 transistors, respectively. Also in the proposed design of [25], each one of these gates are implemented with 5 transistors. While in this paper, we used 4 and 3 transistors for implementing these gates respectively.

Finally, we used these structures for presenting a hybrid design of carry look ahead adder (CLA) that is shown in Fig. 4. As it is shown in Fig. 4, each stage of the proposed CLA is implemented by 25 transistors. Therefore, a 4-bit CLA is proposed with 100 transistors. While, the conventional CLA[26] and Hybrid CLA circuits based on the design presented in [25] use 170 and 138 transistors. So, the proposed design reduces the number of transistors (chip area) by a factor of 44% and 27%, respectively. This reduction is due to the use of full-swing AND and OR gates with smaller area, which will finally lead to a reduction in power consumption and delay of the proposed circuit

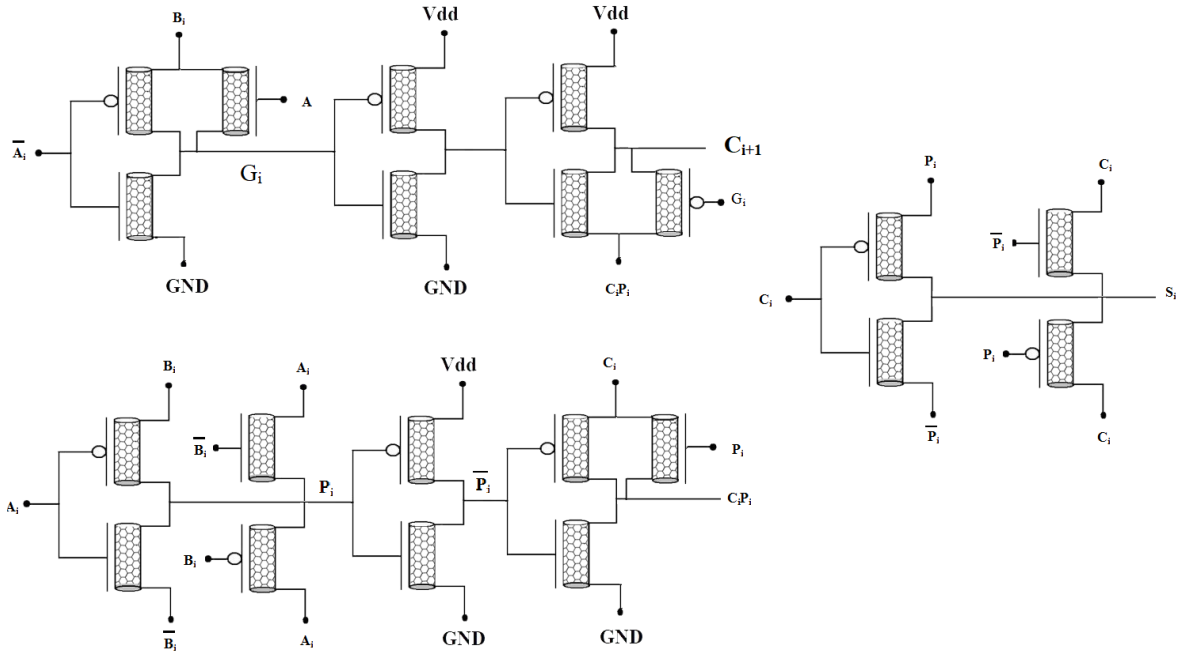


Fig. 4. The proposed circuit of CLA.

4. SIMULATION RESULTS AND COMPARISON

The proposed CLA design is simulated in HSPICE, using the Stanford CNFET model parameters which are summarized in Table. 3.

The input signals Ai, Bi (i=0, 1, 2, 3) and C0 (input carry) are shown in Fig. 5, where the full-swing simulated output signals Si and Ci are also shown. Furthermore, the performance of the proposed CLA design is compared with other reported designs in Table. 4. It is worth noting that, the proposed CLA design as well as other previously reported CLA designs [23] are simulated under the same circuit simulation conditions and the simulation results for the main performance parameters of power consumption, delay and PDP at 200 MHz clock frequency, 0.6V supply and 1fF load capacitance are summarized and compared in Table. 4.

Table 3. The CNFET parameters definitions and values used for circuit simulations

Device parameter	Description	Value
Lch	Physical channel Length	32 nm
Lss	The length of doped CNT source-side extension region	32 nm
Ldd	The length of doped CNT source-side extension region	32 nm
Lgeff	The mean free path in the intrinsic CNT channel	100 nm
pitch	The distance between the centers of two adjacent CNTs within the same device	20 nm
tox	The thickness of high-k top gate dielectric material	4 nm
csub	The coupling capacitance between the channel region and the substrate	40 aF/um
Efi	The fermi level of the doped S/D tube	6 eV

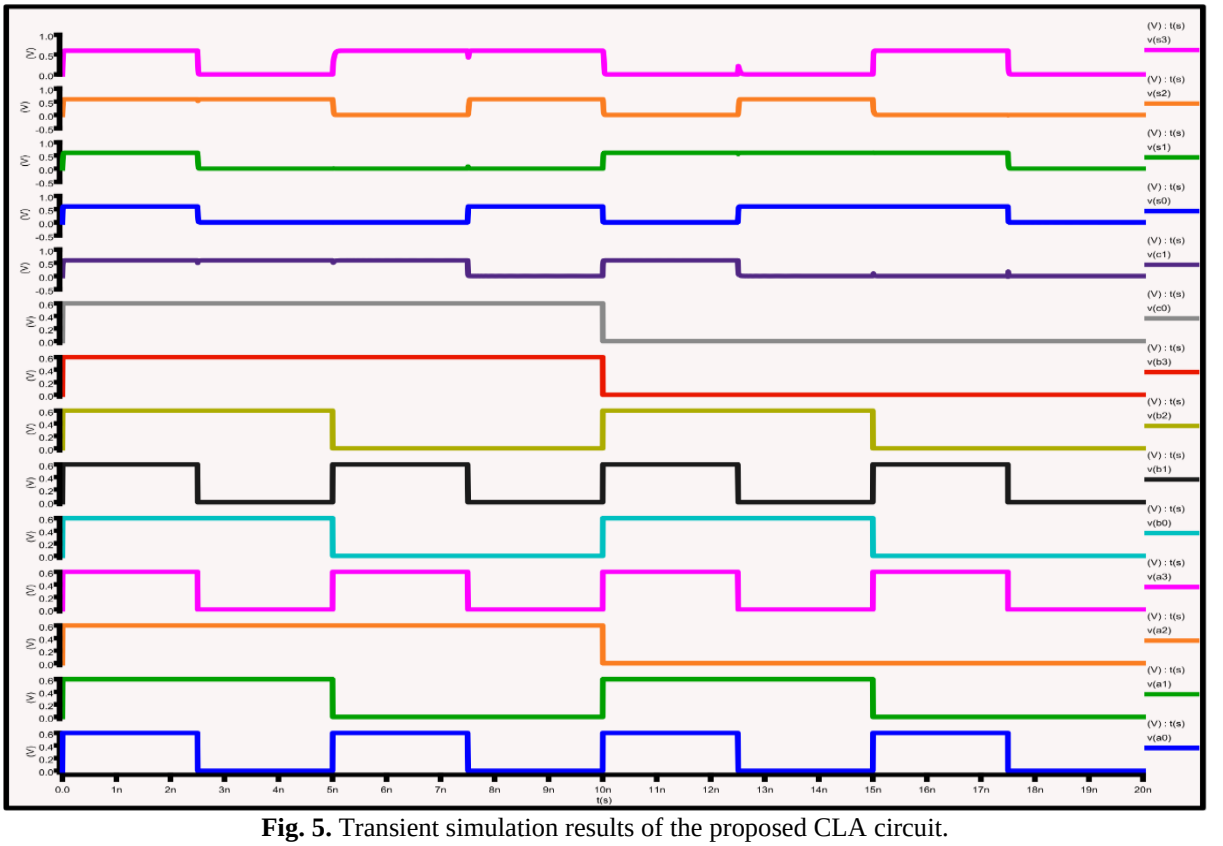


Fig. 5. Transient simulation results of the proposed CLA circuit.

Table 4. Performance comparison of the proposed CLA design and previous designs.

Design	Power (µw)	Delay (Psec)	PDP (aJ)	Transistor count
Conventional CLA [26]	1.15	21.62	2.4863	170
Hybrid GDI CLA [25]	0.948	18.032	1.7094	138
Proposed design	0.848	15.99	1.3559	100

As it is obvious in Table. 4, the proposed CLA circuit has the minimum values of power consumption, delay and PDP parameters in comparison with other reported designs. This improvement is achieved due to the reduction in the number of transistors in the carry generate and propagate structures that led to the reduction of the CLA area and power consumption.

Fig. 6, shows the Comparison of the power consumption, delay and PDP of proposed CLA design with previous CLA designs. As it is clear in Fig. 6a, the proposed design improves the power consumption by a factor of **26%** and **10%** in comparison with conventional and hybrid GDI CLA [25], respectively. Also, it can be seen in Fig. 6b, that the proposed design improves the delay value by a factor of **26%** and **11%** in comparison with the conventional and hybrid GDI CLA [25], respectively. Moreover, as it is clear in in Fig. 6c, the PDP parameter for the proposed circuit is effectively improved by a factor of **45%** and **20%** in comparison with the conventional and hybrid GDI CLA designs [25], respectively. It is worth mentioning that, this improvement is resulted due to the reduction of the number of transistors by using combinational GDI full-swing gates in a CLA structure [20], [24]. Furthermore, the number of tubes (N), is one of the important factors that affects the values of the proposed circuit performance parameters such as: power consumption, delay and PDP. Therefore, the simulation results of the proposed design due to changes in the number of nanotubes (N) are carried out and reported in Fig. 7.

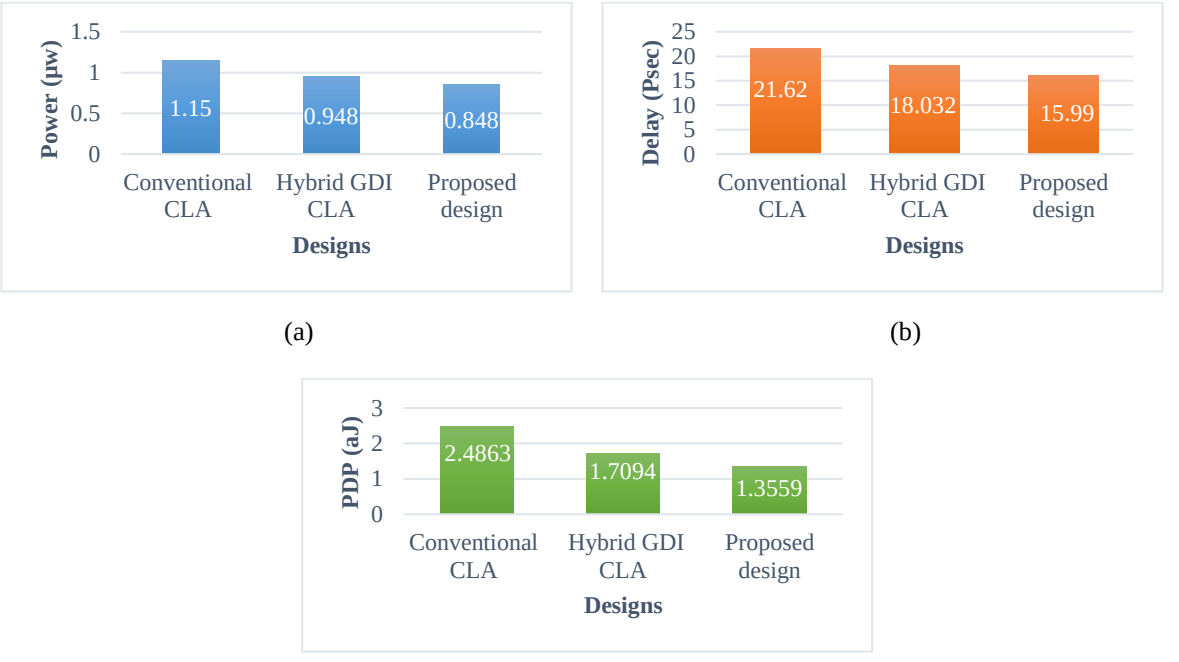


Fig. 6. Performance comparison of the proposed design and other designs a) Power, b) delay and c) PDP.

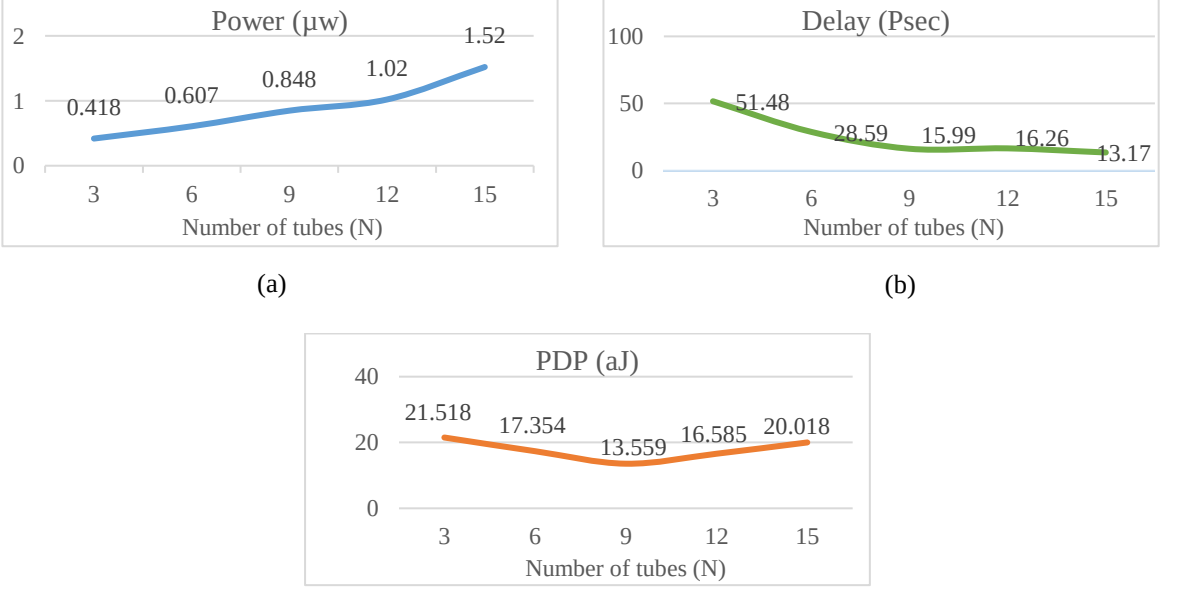
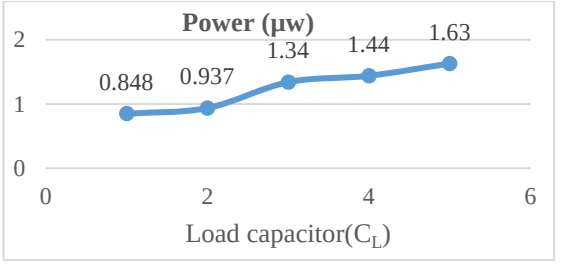


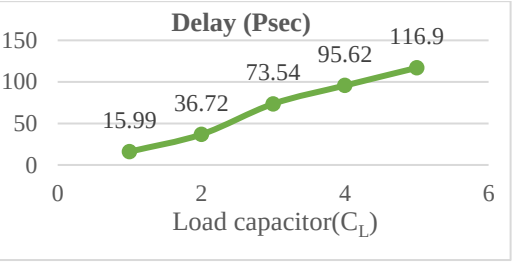
Fig. 7. Effect of changes in the number of tubes on the major performance parameters a) Power, b) delay and c) PDP.

However, as it is clear in Fig. 7, when N=9, the proposed circuit has lowest value of PDP parameter in comparison with other values of the number of tubes N, however, it has a better delay parameter than the other values 3, 6 and 12. Furthermore, the load capacitance has also an important impact on the major performance parameters such as: delay, PDP and dynamic power consumption. Therefore, variations of the performance parameters due to the changes in the value of the load capacitance are analyzed and simulated in Fig. 8. As it is

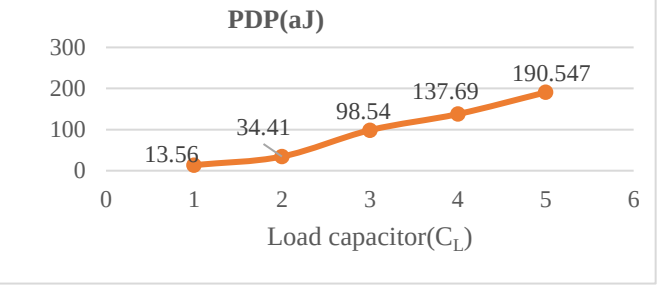
clear in Fig. 8, increasing the value of the load capacitor (C_L), leads to an increase in the power consumption and delay values of the proposed CLA that finally results in an increasing value of PDP parameter. Moreover, the temperature performance simulation results of the proposed circuit are shown in Fig. 9



(a)

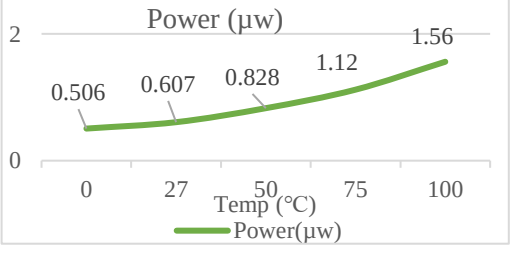


(b)

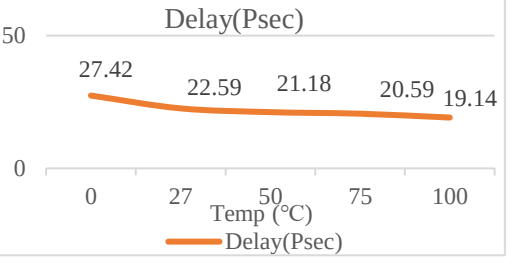


(c)

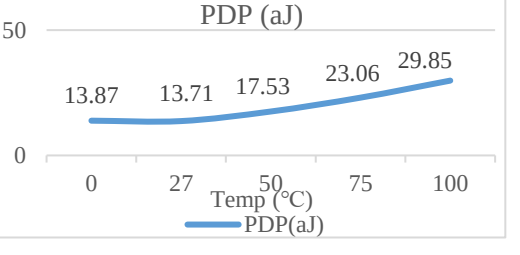
Fig. 8. Effect of the load capacitor variations on the power consumption value on a: Power, b: delay and c: PDP parameters.



(a)



(b)



(c)

Fig. 9. Temperature performance simulation of a) Power consumption, b) delay and c) PDP parameters.

As it is obvious in Fig.9, with an increase in the operating temperature, the power consumption as well as the PDP parameter increases, while the delay value of the proposed CLA decreases.

5. CONCLUSIONS

In this paper, a new low-power and area efficient CLA circuit in CNFET technology based on the full-swing GDI logic style is designed and simulated based on the combination of GDI implemented carry-generate and carry-propagate logic functions respectively. As it is shown in the paper, the proposed design can be considered as an area efficient CLA in which the power consumption is significantly reduced while the speed of the circuit is also improved that leads to the minimum PDP value for the proposed circuit in comparison with other reported designs. Furthermore, the proposed circuit is simulated in HSPICE using 32nm CNFET technology parameters.

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