

# A Multiplier-Less Discrete Cosine Transform Architecture Using a Majority Logic-Based Approximate Full Adder

Elham Esmaeili, Ph.D. Student<sup>1</sup>  | Farshad Pesaran, Assistant Professor<sup>2\*</sup>  | Nabiollah Shiri, Assistant Professor<sup>3</sup> 

<sup>1</sup>Department of Electrical Engineering, Shiraz Branch, Islamic Azad University, Shiraz, Iran, [elham.esmaeili421990@gmail.com](mailto:elham.esmaeili421990@gmail.com)

<sup>2</sup>Department of Electrical Engineering, Shiraz Branch, Islamic Azad University, Shiraz, Iran, [farshad.pesaran@iau.ac.ir](mailto:farshad.pesaran@iau.ac.ir)

<sup>3</sup>Department of Electrical Engineering, Shiraz Branch, Islamic Azad University, Shiraz, Iran, [na.shiri@iau.ac.ir](mailto:na.shiri@iau.ac.ir)

#### Correspondence

Farshad Pesaran, Assistant Professor of Electrical Engineering, Shiraz Branch, Islamic Azad University, Shiraz, Iran, [farshad.pesaran@iau.ac.ir](mailto:farshad.pesaran@iau.ac.ir)

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#### Abstract

This paper proposes a new approximate full adder (FA) based on the majority logic (ML) concept. The fundamental structure of the ML concept is a 3-input majority voter and is widely utilized in digital arithmetic cells. The ML-based proposed FA works at low power, small delay, and low power-delay-product (PDP). The carbon nanotube field-effect transistor (CNTFET) technology lowers the FA power, while the gate diffusion input (GDI) technique is used as the main technique. The swing issue of the GDI technique is resolved by the dynamic threshold (DT) technique. Compared with its exact circuit, the proposed FA saves 2 majority gates, 3 inverters, and a 4.02 ns delay. In the proposed FA, the PDP is improved by 53.73%. The product of the PDP and the normalized mean error distance (NMED) is called PDPE, and in the presented FA, it is reduced by 9.50%. Moreover, the proposed FA is embedded into a multiplier-less discrete cosine transform (DCT) design, which is an appropriate circuit for very large-scale integration (VLSI) systems. The 8-input DCT architecture consumed 2.2321 mW of power for each DCT operation. Also, the circuit has better performance in terms of PDP-area-product (PDAP). The results of DCT implementations confirm the efficiency of the FA.

**Keywords:** Approximate Full Adder, Majority Logic, Discrete Cosine Transform (DCT), Multiplier-Less DCT.

#### Highlights

- A new approximate full adder (FA) based on the majority logic (ML) concept is proposed.
- By reducing number of majority gates and removing inverter, power and delay of the purposed circuit is reduced.
- The carbon nanotube field-effect transistor (CNTFET) technology and gate diffusion input (GDI) technique are used to implement the proposed circuit.
- To compensate the outputs voltages the dynamic threshold (DT) technique is used.
- The proposed FA is embedded into a discrete cosine transform (DCT) structure.