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Research Article

Low Latency and Power Efficient Reversible Full Adder based on Toffoli Gates

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Abstract

The reversible circuits are useful in energy-saving applications because of their unique features. Hence, using 32 nm carbon nanotube field-effect transistor (CNTFET) technology and relying on Toffoli's reversible gates, a new full adder (FA) circuit is presented. The proposed circuit has 4 basic Toffoli gates and 18 transistors. 3 of the 4 gates have the same transistor schematic with a constant-ON transistor, but the remaining gate has only two transistors. The proposed circuit has 3 constant inputs and 4 garbage outputs. As a new method, in the proposed circuit, only one type of reversible gate is used. The results show the superiority of the proposed FA in terms of power consumption and energy dissipation. By implementing the proposed FA and other circuits in a 4-bit and 8-bit ripple carry adder (RCA), the proposed circuit shows improvements by 6.83% and 11.25% in terms of power and energy, respectively, compared to the main competitor. Also, in an 8-bit RCA, the proposed FA has a 2% saving compared to the nearest competitor and 27% compared to the worst circuit in terms of the power-delay-area-product (PDAP). These results show the designed FA as a favorable option for complex structures with high-order bits.

Keywords: Full adder, Toffoli gate, Reversible design, Low power, High speed, Ripple carry adder.

Highlights

- Covering the lack of transistor design of reversible full adders based on CNTFET technology with a channel length of 32 nm.
- Design of a new Toffoli gate (TG) and its usage in the proposed full adder for circuitry performance improvement in terms of power and delay.
- Use of only one type of reversible gate, Toffoli gate (TG), in the design of the proposed full adder.
- Obtaining the proposed full adder with high precision in terms of output voltage generation for use in various high-speed and frequency-dependent applications.

Citation: (in Persian).