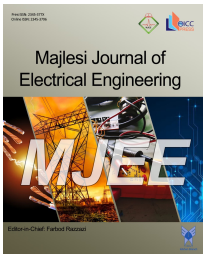


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# A CMOS 65 nm on-chip RF inductor with hybrid spiral-meander layout optimization and ferroelectric stack-up integration for Q-factor enhancement

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**Abstract:**

On-chip inductors are crucial for enhancing the functionality of microelectronic devices, particularly in wireless communication. Still, traditional designs often lead to increased chip size and reduced performance due to their bulkiness and integration challenges. By utilizing an electromagnetic (EM) simulation tool, this research presents a novel on-chip inductor design optimized for 65 nm CMOS technology, achieving an inductance of 3.2 nH with a Q-factor of 15.31 at 1.7 GHz. The primary contributor to the Q-factor enhancement is the layout optimization techniques, which improve the Q-factor by approximately 21%. Additionally, further improvements in inductance and Q-factor are achieved by integrating Nickel Zinc Cobalt-based ferroelectric liquid materials into the simulation stack-up layer. This material stack-up serves as a secondary contributor, enhancing the magnetic properties of the inductor and increasing the Q-factor to 15.83 which is an additional 6% improvement over the proposed design. The proposed layout optimization and material innovations demonstrate the potential for achieving higher inductance values and Q-factors, effectively addressing the limitations of conventional methods. The results highlight the feasibility of incorporating advanced materials in on-chip inductor design, paving the way for next-generation RF integrated circuits that meet the growing demands for miniaturization and energy efficiency in modern electronics.

**Keywords:** Complementary metal oxide semiconductor; Inductor; Quality factor; Layout optimization; Ferroelectric

## 1. Introduction

In wireless communication, capacitors and inductors are frequency selection's most significant reactive components. Out of these two reactive components, the inductor occupies a significant size of the entire chip area. As a result, any RF circuits containing passive inductors such as the voltage-controlled oscillator (VCO) [1], low-noise amplifier (LNA) [2, 3], filter, and power dividers consume immense chip size. The realization of high-quality factor (Q-factor) on-chip inductor is important for several efficient RF circuit designs such as impedance matching networks, LC resonators, filters, and power combiners and dividers [4]. On-chip inductor design and manufacturing saw tremendous advancements in the 1990s and 2000s. As one of the very latest findings, an LC-VCO architecture incorporating a novel tunable active inductor using 90 nm gpdk technology for wireless communication systems is proposed which achieved the Q-factor of 3040 at 8.1 GHz and a low inductance of 2.26 nH in simulation [5]. To improve the performances, researchers experimented with various materials and layout shapes. Researches are now focusing in developing tunable inductors which are able to fine-tune the inductance value after fabrication, offering flexibility and reliability [6]. Thicker metal layers are typically used to sustain high current flow and to achieve high Q-factor. The Q-factor was increased by using wider metal layers, which reduce the series resistance of the inductor. The design

of multi-layer inductors was another implemented concept accomplished by vertically stacking several metal layers to achieve larger inductance values without appreciably expanding the area. Patterned ground shielding (PGS) insertion was another implementation that integrated a shield of metal patterns between the inductor and the silicon substrate to reduce substrate losses and increase the Q-factor. However, the optimal PGS solutions and corresponding suitable frequency ranges for inductors of different inductances are still being researched [7]. Extensive analysis revealed that the shield can improve the Q-factor only of the inductor operated at the lowest frequency [8]. Deep Reactive Ion Etching (DRIE) of silicon enables the microfabrication of high-aspect-ratio structures (HARS), which, in turn, permits the fabrication of devices able to span from 100 to 1000 μm [9].

Today, high-aspect-ratio structures are made possible by sophisticated semiconductor production methods like DRIE and electroplating, which further enhance the performance of on-chip inductors. These methods reduced parasitic effects and provided more control over the geometry of the inductor. It was possible to produce RFICs with integrated passive components in large quantities. This integration made the widespread use of wireless technologies like Wi-Fi, Bluetooth, and cellular communication possible. Recently, more complex on-chip inductors have been made possible by applying microelectromechanical systems (MEMS) technology [10]. By suspending the inductor structure above the substrate, MEMS-based inductors can achieve greater Q-factors and inductance values while minimizing substrate losses. Due to material science and nanotechnology developments, novel materials, including graphene and other 2D materials, are being investigated for on-chip inductors [11]. Also, materials such as FeCoB films with a self-biased ferromagnetic frequency up to 21 GHz are deposited on Si substrates using the compositional gradient sputtering method as a magnetic underlayer to realize an on chip inductor [12]. These materials can potentially revolutionize the design of on-chip inductors due to their improved electrical characteristics.

Predicting the behaviour of on-chip inductors in integrated circuits can be done more simply and insightfully with the help of analytical models. These models compromise computational efficiency and accuracy because they rely on mathematical equations derived from basic concepts in circuit theory and electromagnetics. They are especially helpful for understanding inductor behaviour qualitatively and in the early design phases. On-chip inductors typically consist of a spiral-shaped metal trace and their performance is characterized by key parameters like inductance ($L$), Q-factor ($Q$), and self-resonant frequency (SRF). Analytical models aim to express these parameters regarding the inductor's geometric dimensions and material properties [13, 14]. It is possible to determine the inductance of an on-chip spiral inductor by applying simplified formulas that come from magnetic field theory. The modified Wheeler formula [13], which is frequently applied to square spiral inductors, is:

$$L = \frac{K_1 d_{\text{avg}} n^2 \mu}{1 + k_2 \rho} \tag{1}$$

where $L$ is the inductance in Henries (H), $\mu$ is the permeability of free space (Wb/A·m) ($4\pi \times 10^{-7}$ H/m), $n$ is the number of turns in the spiral. $\rho$ is the fill ratio (describes how "tightly packed" the spiral is), For an example, a smaller fill ratio (more tightly packed turns) increases inductance due to stronger magnetic coupling. $d$ is the diameter of the inductor, and $K$ is the empirical fitting constants that depend on the shape of the spiral. This calculation simplifies the detailed magnetic field interactions inside the spiral, yet yields a decent first-order estimate of the inductance.

The Q-factor [15], which is the ratio of the inductor's reactance to resistance at a specific frequency, is a measurement of its efficiency:

$$Q = \frac{2\pi f L}{R} \tag{2}$$

where $Q$ is the quality factor of the inductor, $f$ is the frequency, $L$ is the inductance, and $R$ series resistance of the inductor, which includes both the resistance of the metal traces and additional losses such as substrate losses.

$$R = \frac{\rho L}{\omega t} \tag{3}$$

where $\rho$ is the resistivity of the metal, $L$ is the total length of the spiral trace, $\omega$ is the width of the metal trace and $t$ is the thickness of the metal layer.

For higher accuracy, the Q-factor calculation may also include effects like the skin and proximity effects, which increase the effective resistance at higher frequencies. Parasitic capacitance between the spiral's turns and between the inductor and the substrate beneath it impacts on-chip inductors. It is possible to model this capacitance using basic parallel-plate capacitor formulas.

$$C_{sub} = \varepsilon_{ox} \frac{A}{d_{ox}} \tag{4}$$

where $C_{sub}$ is the substrate's capacitance, $\varepsilon_{ox}$ is the oxide layer's permittivity, $A$ is the area of the inductor, and $d_{ox}$ is the thickness of the oxide layer.

The self-resonant frequency is the frequency at which the inductive reactance is cancelled out by the parasitic capacitance, leading to resonance:

$$f_{sr} = \frac{1}{2\pi\sqrt{L - C_{\text{tot}}}} \tag{5}$$

where $C_{\text{tot}}$ is the total parasitic capacitance including both inter-turn and substrate capacitances.

Based on the inductor's design and material parameters, analytical models of on-chip inductors offer a helpful tool for calculating the inductance, Q-factor, and SRF. Despite their shortcomings, these models are frequently employed in the preliminary stages of integrated circuit design. They give designers a rapid and intuitive grasp of inductor performance before advancing to more in-depth simulations or empirical techniques.

Thus, this paper presents a custom on-chip inductor design with optimized layout geometry for 65 nm CMOS technology using an EM simulation tool. The designed inductor attains an inductance of 3.2 nH and a Q-factor of 15.31 at 1.7 GHz. Malaysia's 1.7 GHz frequency band is actively

utilized for mobile cellular services. Specifically, the band from 1.710 GHz to 1.785 GHz is paired with 1.805 GHz to 1.880 GHz to form the 1.8 GHz band, commonly called the GSM 1800 or DCS 1800 band. This band supports various generations of mobile technologies, including 2G (GSM), 3G (UMTS), and 4G (LTE). Enhanced performance of the inductor is achieved by incorporating Nickel-Zinc-Cobalt-based ferroelectric liquid materials into the simulated stack-up layer, resulting in a Q-factor of 15.83 due to improved magnetic properties of the inductor. The enhanced performance of the custom-designed inductor is compared with the conventional inductor performance of the foundry. The proposed methodology can be varied by implementing the layout and stack-up modification according to the frequency of interest or the technology nodes.

## 2. Design methodology of the custom on-chip inductor

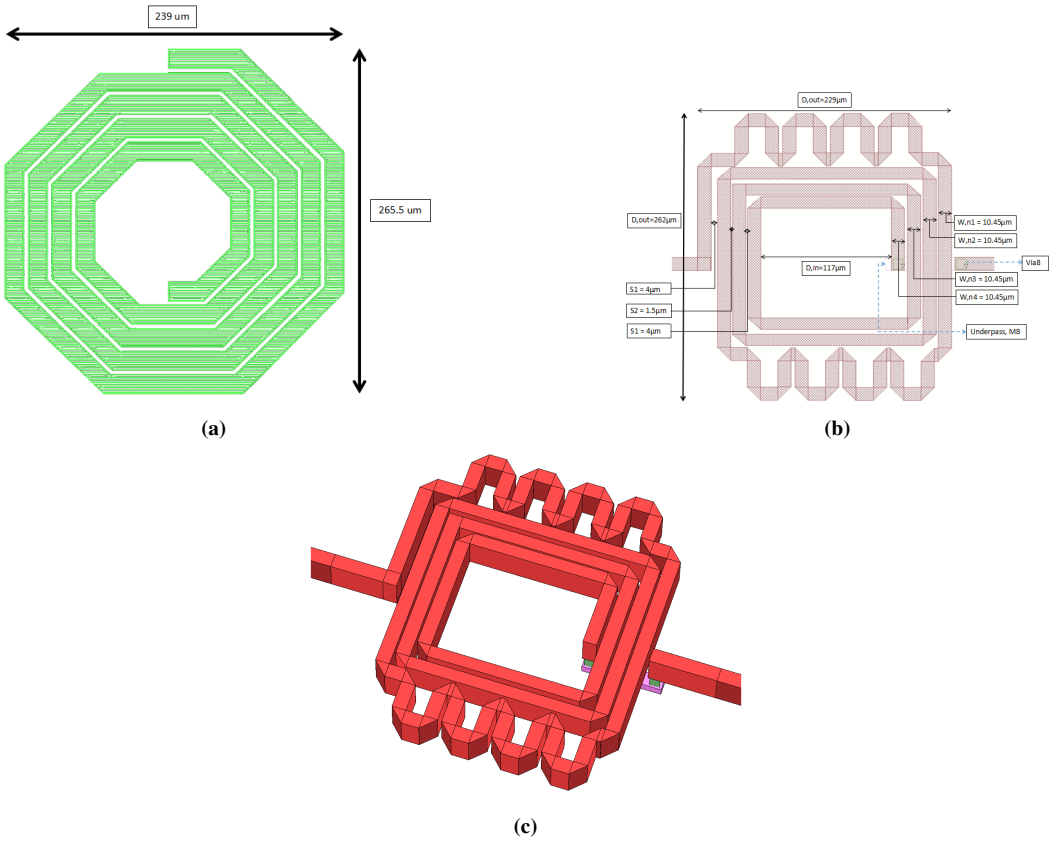
### 2.1 Layout optimization

The proposed custom inductor was designed using Sonnet EM software in 65 nm CMOS technology with a nine-metal layers process option. From the foundry's process design kit (PDK), the inductor operating at 1.7 GHz with the best Q-factor has four turns with an area consumption of $239 \times 265.5$ µm$^2$. The inductor achieves an inductance of 3.2 nH. Taking this as a baseline, the study is conducted by selecting a 3.2 nH value of inductance, and the aim is to enhance the inductance and Q-factor with an equal or smaller form-factor that occupies the area on-chip. The custom inductor illustrated in Fig. 1a in 2D and 1b in 3D is designed with four turns with fixed metal widths of 10.45 µm with alternate spacing between the turns, which is 1.5, 4, and again 1.5 um. As depicted in Fig. 1, 2 sides of the 4$^{\text{th}}$ turn of the inductor are designed in meander zig-zag form, enhancing the inductance of the proposed inductor. The designed inductor consists of integrated spiral and meander shapes, enhancing the inductance for a given area, and their related derivation is given in equation (6). The inner diameter ($D_{\text{in}}$) and outer diameter ($D_{\text{out}}$) are 117 µm and 229 µm, respectively. The metal strip of the inductor is traced with thick top metal, in this case, Metal 9, which has a conductivity of 5.8e7 S/m and a thickness of 3.4 µm. The underpass is traced with Metal 7, which has a conductivity of 5.05e7 S/m and a metal thickness of 0.9 µm. Via between the metals has a conductivity of 2.23e7 S/m.

$$L = \left(\sum_i L_i + \sum_{i \neq j} M_{ij}\right)_{\text{spiral}} + \left(\sum_i L_i + \sum_{i \neq j} M_{ij}\right)_{\text{meander}} \quad (6)$$

where $Li$ is the self-inductance of segment $i$, $M_{ij}$ is the mutual inductance between segments $i$ and $j$, and $ij$ are the Indices of the segments.

The total inductance ($L$) of this composite on-chip inductor made up of both a spiral and meander structure is represented by equation (6). It is derived from the conventional inductance formula, which takes into account both the mutual inductance between various segments and the self-inductance of each segment. The meander section, which maximizes layout efficiency, is represented by the second term, whereas the first term accounts for the induc-




**(a)** **(b)** **(c)**

**Figure 1.** (a) 2d view of the conventional inductor (b) 2D and (c) 3D views of the proposed custom Inductor.

tance of the spiral section, where closely packed turns boost mutual inductance. These two contributions add up to the total inductance because inductance is additive.

### 2.2 New material stack up

Liquid ferroelectric materials were stacked up on the top metal layer and simulated in the Sonnet EM simulation tool to study the impact of the materials on the inductor performance [16]. A liquid ferroelectric material layer is added at the same stack-up level and above the top metal layer. Fig. 2 shows an example of the stack-up technology utilized to simulate the inductor after adding the ferroelectric liquid material. The ferroelectric material is positioned on the uppermost metal layer in the dielectric stack-up to improve the performance of the inductor. By altering the electric field distribution, its high permittivity raises the effective inductance, and its special dielectric qualities lower energy losses, improving the Q-factor. An efficient method for maximizing inductor performance across a range of frequencies, this location allows for both inductance adjustment and loss minimization. The material that was studied and simulated for this purpose is Nickel-Zinc-Cobalt ($Ni_{0.5}Zn_{0.3}Co_{0.2}In_xFe_{(2-x)}O_4$) [17]. For this study, various ferroelectric materials were studied, such as Barium Strontium Titanate (BST), Lead Zirconate Titanate (PZT), and other MnZn-based materials.

A study reported a dielectric constant of 283 at room temperature for BST thin films fabricated on titanium substrates [18]. BST is primarily recognized for its dielectric properties and is generally considered non-magnetic. Therefore, its relative permeability ($\mu_r$) is approximately 1, similar to that of free space. Temperature affects BST's dielectric characteristics. The temperature range throughout which BST retains stable dielectric behavior can be controlled by varying the barium-to-strontium ratio, which enables tweaking of the Curie temperature [19]. BST has a lesser magnetic permeability than NiZnCo despite being a tremendous ferroelectric material for tunability. This restricts BST's potential to increase inductance in specific uses.

In contrast to NiZnCo, PZT is another ferroelectric material with a high permittivity, although it often experiences more significant losses at higher frequencies, especially dielectric losses. The value of dielectric constant ($\varepsilon_r$) at 1 KHz is 515.492 and value of dielectric loss ($\tan\delta$) is found to be 0.005 at same frequency. Measurement at high temperatures permit to determine, from the maximum of $\varepsilon_r(T)$, the Curie temperature $TC = 380\ ^\circ$C of the ferroelectricparaelectric phase transition of PZT ceramic [20]. However, PZT is more brittle and difficult to incorporate into semiconductor processes. High magnetic permeability and ferroelectric

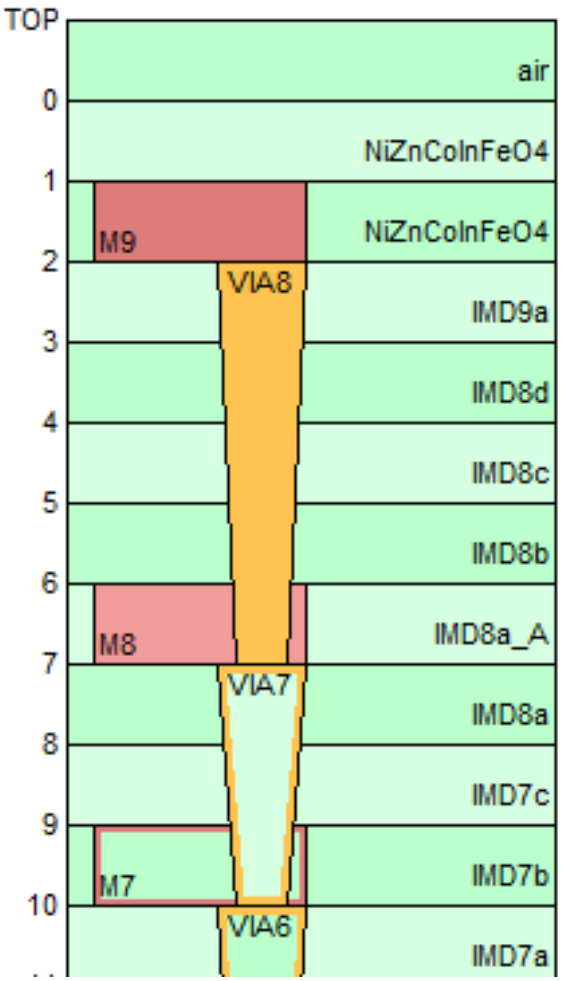



**Figure 2.** Dielectric stack-up of the CMOS 65 nm process with inductor metals and ferroelectric liquid materials.

characteristics combine in NiZnCo-based materials to produce improved inductance performance without appreciably lowering the Q-factor. For on-chip inductors that need a high inductance density in a small package, this is very advantageous.

In conclusion, NiZnCo liquid ferroelectrics are an excellent option for raising the Q-factor of inductors, particularly in the targeted 1.7 GHz frequency, because they provide optimum permeability, low dielectric losses, temperature stability, and integration capacity. This ferroelectric liquid material has a dielectric constant of 10 and a magnetic permeability of 15.2. Adding this material into the dielectric stack-up enhances the inductance and Q-factor of the designed inductor, as related to the derivation in equation (7). Wheeler's equation now has a modified permeability, $\mu = \mu_0\mu_r$, where $\mu_0$ is the permeability of free space, and $\mu_r$ is the permeability of the ferroelectric material. Ferroelectric liquid materials have a higher relative permeability, $\mu_r$, than air ($\mu_r = 1$). When the ferroelectric liquid is introduced above the planar inductor, the effective permeability of the medium surrounding the inductor increases since inductance is proportional to $\mu$, as shown in equation (7).

$$L = \frac{K_1 d_{avg} n^2 \mu_0 \mu_r}{1 + k_2 \rho} \tag{7}$$

The permeability of ferroelectric liquid is also a function of frequency and generally expressed as a complex quantity, $\mu = \mu' - j\mu''$ where $\mu'$ is the real part of permeability associated with energy storage in the material. At the same time, $\mu''$ is the imaginary part of permeability related to energy losses [24].

## 3. Results and discussion

At the targeted frequency of 1.7 GHz, the simulated Q-factor achieved by the proposed inductor is 14.8 with an inductance of 3.16 nH. The area consumed is $229 \times 262$ $\mu m^2$, less than the size of the conventional inductor from the foundry. Compared with the conventional inductor from the foundry, the Q-factor is enhanced by 21.31%, which caters to a 2.6 improvement from the initial value of 12.2. Fig. 3a and 3b depict the simulated inductance and Q-factor values across the frequency compared to the conventional inductor.

It can be observed in Fig. 3a that at the intended frequency (1.7 GHz), the inductance value is maintained with a marginal drop, while about a 3 GHz increase in the SRF is achieved. Increasing the inductor's self-resonant frequency (SRF) would enable it to function inductively across a broader range of frequencies, enhancing its usefulness in high-frequency circuits. Both inductors show a steady initial inductance at lower frequencies. However, the custom inductor shows much smoother behavior with a lower inductance peak. Beyond SRF, custom inductors also demonstrate less negative inductance, suggesting better control over parasitic effects. In Fig. 3b, the custom inductor achieves a higher Q-factor, reflecting reduced resistive losses and better energy storage efficiency at 1.7 GHz. Furthermore, the inductance and Q-factor are further boosted by employing the ferroelectric material on top of the inductor. Fig. 4a shows the inductance value achieved, while Fig. 4b shows the proposed inductor's Q-factor performance compared with the conventional inductor.

The ferroelectric liquid material enhances the Q-factor by another 1.03 value, which sums up to 3.63 of improvement in the Q-factor compared to the conventional inductor. The total improvement in Q-factor is 29.75% for the proposed inductor. The ferroelectric liquid material also increases the inductance value of the designed inductor by 1.64 nH. The absolute improvement noted in the inductance (1.64 nH) directly corresponds to the material's permeability, as shown in (7). The primary factor contributing to the Q-factor improvement is the layout optimization techniques, which enhance the Q-factor by approximately 21%. Additionally, the secondary contributor is the novel material stack-up, which further increases the Q-factor by approximately 6% from the proposed design. The improvement in inductance without jeopardizing the Q-factor for the given form factor indicates that the size of the conventional on-chip inductor can be reduced, especially for low-frequency applications that require large inductors. Meanwhile, Table 1 summarizes its performance.

In addition, the designed custom inductor is also compared

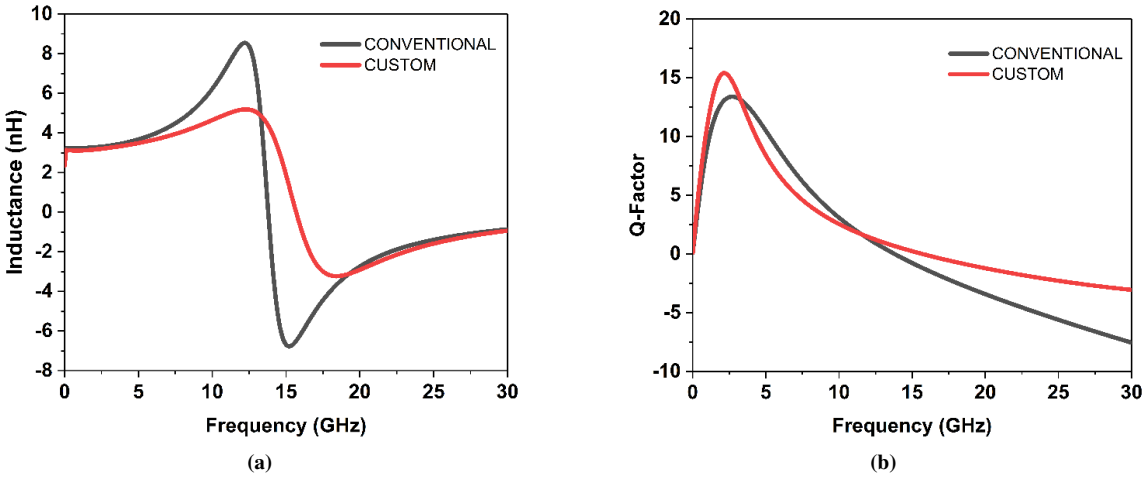



**Figure 3.** The (a) inductance and (b) Q-factor values of the custom inductor and the conventional inductor.

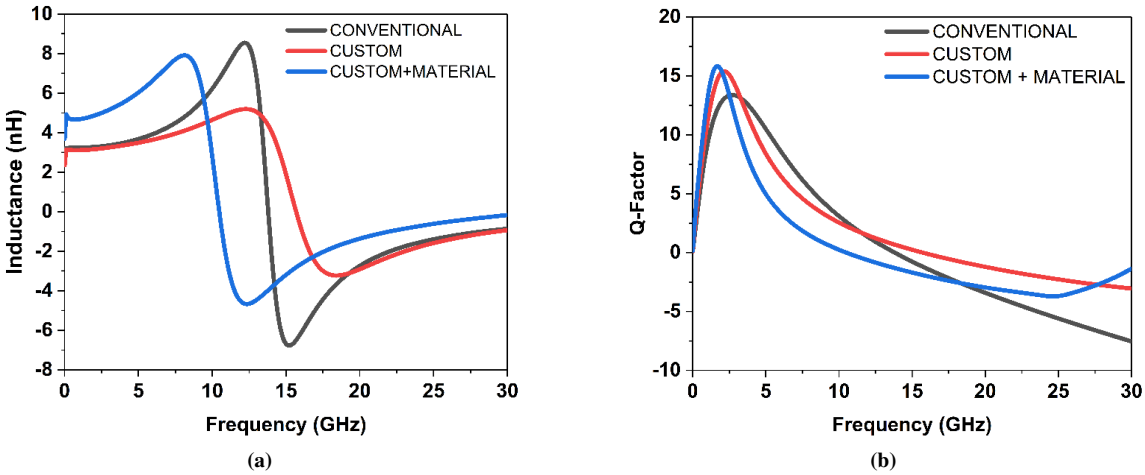



**Figure 4.** The (a) inductance and (b) Q-factor values of the inductor with ferroelectric material addition.

with the current state-of-the-art one, as delineated in Table 2. Table 2 compares inductance, operating frequency, and quality factor (Q-factor) for various inductor designs employing layout optimization approaches, with the proposed design featuring both layout and material optimization. The mentioned designs in [19, 20, 24] utilize layout optimization to optimize the performance of on-chip inductors by altering their physical structure to minimize parasitic losses and improve overall efficiency. The proposed custom design had a higher Q-factor, which suggests that the layout and ferroelectric material optimization enhance efficiency.

Based on the recently published review papers of on-chip inductors, our proposed design demonstrates a higher Q-factor compared to recent works within the 65 nm technology node, as verified through simulation results [25]. Additionally, in terms of material selection, our design has exhibited superior $Q$ performance relative to many previously reported inductor designs, as supported by the reference [26].

## 4. Conclusion

The proposed custom inductor design was simulated in an EM modeling tool using 65 nm CMOS technology. The optimized layout achieved a Q-factor of 15.31 and an inductance of 3.2 nH at 1.7 GHz. A zigzag meander structure improved $Q$ by minimizing energy losses, optimizing current distribution, and reducing parasitic capacitance. Dispersed conductor routing mitigated substrate coupling and inter-turn capacitance, lowering resistive losses. Enhanced current flow reduced proximity effects and skin-effect-related losses. Alternating trace spacing, while maintaining width, optimized mutual inductance, improved magnetic coupling, and suppressed parasitics. This enhanced high-frequency performance while minimizing eddy current losses. Balancing coupling and loss mechanisms improved efficiency without increasing chip area. Incorporating Ni–Zn–Co-based ferroelectric liquid materials raised $Q$ to 15.83 by increasing dielectric permeability. The results demonstrate that higher inductance and $Q$ are attainable in on-chip inductors. The design and material modifications are scalable to any technology node and frequency range. Metal width, spacing, and turns can be tuned for diverse manufacturing processes. The model, grounded in electromagnetic principles, is technology-independent and EM-simulation compatible. Challenges remain in integrating ferroelectric materials with precise thickness, composition, and crystallinity control in standard foundry flows.

**Table 1.** Performance summary of the proposed inductor in comparison with conventional inductor.

| | Conventional | Custom | Custom + Ferroelectric liquid |
|---|---|---|---|
| Area (μm) | 239 × 265.5 | 229 × 262 | 229 × 262 |
| Frequency (GHz) | 1.7 | 1.7 | 1.7 |
| Inductance (nH) | 3.20 | 3.16 | 4.80 |
| Maximum Q-factor | 12.20 | 14.80 | 15.83 |
| % of $Q$ improved (%) | 21.31% | | 29.75% |

**Table 2.** Performance comparison of the proposed custom inductor with recent state-of-the-art inductors.

| References | Technique used | Inductance (nH) | Frequency (GHz) | Q-factor |
|---|---|---|---|---|
| [21] | Layout optimization | 3.41 | 2.4 | 7.38 |
| [22] | Layout optimization | 3 | 1.8 | 5.23 |
| [23] | Layout optimization | 4 | 2.4 | 12.71 |
| This work | Layout optimization + Material | 4.8 | 1.7 | 15.83 |

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**Authors contributions**
Authors have contributed equally in preparing and writing the manuscript.

**Availability of data and materials**
The data that support the findings of this study are available from the corresponding author upon reasonable request.

**Conflict of interests**
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## References

[1] A. Daghighi and A. R. Neshat-Niko. "**VCO design and simulation using TSMC 0.18 $\mu$m process to meet IEEE802.11a requirements**.". *Majlesi J. Electr. Eng.*, 2(2), 2024.
DOI: https://doi.org/10.1234/mjee.v2i2.56.

[2] F. Shirani Bidabadi and S. V. Mir-Moghtadaei. "**Low power broadband sub-GHz CMOS LNA with 1 GHz bandwidth for IoT application**.". *Majlesi J. Electr. Eng.*, 16(4), 2022.
DOI: https://doi.org/10.30486/mjee.2022.696519.

[3] M. Jalalifar, M. Yavari, and F. Raissi. "**A novel frequency compensation technique in three stage amplifiers with active feedback**.". *Majlesi J. Electr. Eng.*, 4(1), 2024.
DOI: https://doi.org/10.1234/mjee.v4i1.216.

[4] A. Bhaskar, S. Kumar, P. Singh, R. Sharma, and V. Gupta. "**Substrate engineering of inductors on SOI for improvement of Q-factor and application in LNA**.". *IEEE J. Electron Devices Soc.*, 8:959–969, 2020.
DOI: https://doi.org/10.1109/JEDS.2020.3019884.

[5] I. Kadyan, M. Kumar, and A. P. Singh. "**Design and analysis of a novel 90 nm tunable active-inductor with high Q-factor in LC-VCO for C and Ku band**.". *Eng. Res. Express*, 7(1):015372, 2025.
DOI: https://doi.org/10.1088/2631-8695/adbcfb.

[6] N. S. Yusof, M. H. Ibrahim, A. Z. Abidin, and R. M. Sidek. "**Patterned ground shield for inductance fine-tuning**.". *IETE J. Res.*, 68(4):2764–2778, 2020.
DOI: https://doi.org/10.1080/03772063.2020.1726827.

[7] J.-N. Wu, Y.-M. Chang, Z.-Y. Shen, and H.-C. Chen. "**Investigation on CMOS on-chip inductors using various patterned ground/floating shield techniques**.". *Proc. Int. Conf. Electron. Commun., IoT Big Data (ICEIB)*, pages 113–116, 2021.
DOI: https://doi.org/10.1109/ICEIB53692.2021.9686404.

[8] S. Spataro, N. Salerno, G. Papotto, and E. Ragonese. "**The effect of a metal PGS on the Q-factor of spiral inductors for RF and mm-wave applications in a 28 nm CMOS technology**.". *Int. J. RF Microw. Comput.-Aided Eng.*, 30(10), 2020.
DOI: https://doi.org/10.1002/mmce.22368.

[9] N. K.-S. Chen, A. A. Ayon, N. X. Zhang, and S. M. Spearing. Effect of process parameters on the surface morphology and mechanical performance of silicon structures after deep reactive ion etching (drie). *J. Microelectromech. Syst.*, 11(3):264–275, 2002.
DOI: https://doi.org/10.1109/JMEMS.2002.1007405.

[10] O. F. Hikmat and M. S. M. Ali. "**RF MEMS inductors and their applications—A review**.". *J. Microelectromech. Syst.*, 26(1):17–44, 2017.
DOI: https://doi.org/10.1109/JMEMS.2016.2627039.

[11] J. Kang et al. "**On-chip intercalated-graphene inductors for next-generation radio frequency electronics**.". *Nat. Electron.*, 1(1): 46–51, 2018.
DOI: https://doi.org/10.1038/s41928-017-0010-z.

[12] C. Sun et al. "**Inductance and Q-factor of micromagnetic inductor are enhanced by FeCoB films with self-bias**.". *Phys. Status Solidi RRL*, 19(1):2400167, 2025.
DOI: https://doi.org/10.1002/pssr.202400167.

[13] S. Salleh, K. Salleh, M. F. Hashim, and Z. Abd. Majid. "**Design and analysis of 13.56 MHz RFID antenna based on modified Wheeler equation: A practical approach**.". *Proc. Int. Conf. Electron. Devices, Syst. Appl. (ICEDSA)*, pages 326–330, 2010.
DOI: https://doi.org/10.1109/ICEDSA.2010.5503048.

[14] A. Alkasir, S. E. Abdollahi, S. Abdollahi, and P. Wheeler. "**Analytical modeling of self-and mutual inductances of DD coils in wireless power transfer applications**.". *J. Electromagn. Eng. Sci.*, 22(2):162–170, 2022.
DOI: https://doi.org/10.26866/jees.2022.2.r.73.

[15] E. S. Mawuli et al. "**Distributed characterization of on-chip spiral inductors for millimeter-wave frequencies**.". *Proc. IEEE MTT-S Int. Conf. Numer. Electromagn. Multiphys. Modeling Optim. (NEMO)*, pages 1–4, 2020.
DOI: https://doi.org/10.1109/NEMO49486.2020.9343469.

[16] R. Sai, R. D. R. Kahmei, S. A. Shivashankar, and M. Yamaguchi. "**High-Q on-chip C-band inductor with a nanocrystalline MNZN-ferrite film core**.". *IEEE Trans. Magn.*, 55(7):1–4, 2019.
DOI: https://doi.org/10.1109/TMAG.2019.2916699.

[17] A. Saini et al. "**Magneto-dielectric properties of doped ferrite-based nanosized ceramics over very high frequency range**.". *Eng. Sci. Technol. Int. J.*, 19(2):911–916, 2016.
DOI: https://doi.org/10.1016/j.jestch.2015.12.008.

[18] M. Wang, W. Li, X. Zuo, W. Zhu, and G. Zhang. Structure and dielectric properties of barium strontium titanate ferroelectric thin film prepared by dc micro-arc oxidation. *Appl. Phys. A*, 126:1–8, 2020.
DOI: https://doi.org/10.1007/s00339-020-03937-0.

[19] O. M. Hemeda, B. I. Salem, and M. Mostafa. "**Structural and electric properties of strontium barium titanate prepared by tartrate precursor method**.". *Eur. Phys. J. Plus*, 135(1):1–15, 2020.
DOI: https://doi.org/10.1140/epjp/s13360-019-00021-2.

[20] P. Goel, K. L. Yadav, and A. R. James. "**Double doping effect on the structural and dielectric properties of PZT ceramics**.". *J. Phys. D: Appl. Phys.*, 37(22):3174, 2004.
DOI: https://doi.org/10.1088/0022-3727/37/22/019.

[21] H.-H. Chen and Y.-W. Hsu. "**Analytic design of on-chip spiral inductor with variable line width**.". *Electronics*, 11(13):2029, 2022.
DOI: https://doi.org/10.3390/electronics11132029.

[22] A. Thakur and S. Chatterjee. "**Design of a monolithic inductor and its influence on the oscillator design**.". *IETE J. Res.*, 68(3): 2238–2245, 2019.
DOI: https://doi.org/10.1080/03772063.2019.1696715.

[23] H. Bouyghf, B. Benhala, and A. Raihani. Analysis of the impact of metal thickness and geometric parameters on the quality factor-q in integrated spiral inductors by means of artificial bee colony technique. *Int. J. Electr. Comput. Eng.*, 9(4):2918–2931, 2019.
DOI: https://doi.org/10.11591/ijece.v9i4.pp2918-2931.

[24] S. B. Cho, D. H. Kang, and J. H. Oh. "**Relationship between magnetic properties and microwave-absorbing characteristics of NiZnCo ferrite composites**.". *J. Mater. Sci.*, 31:4719–4722, 1996.
DOI: https://doi.org/10.1007/BF00366375.

[25] R. Ondica et al. "**An overview of fully on-chip inductors**.". *Radioengineering*, 32(1):11, 2023.
DOI: https://doi.org/10.13164/re.2023.0011.

[26] H. Chen et al. "**Integrated tunable magnetoelectric RF inductors**.". *IEEE Trans. Microw. Theory Techn.*, 68(3):951–963, 2020.
DOI: https://doi.org/10.1109/TMTT.2019.2957472.