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ORIGINAL ARTICLE

Design of magnetic dipole based 3D integration nano-circuits for future electronics application

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Abstract

Nano Magnetic Logic (NML) has been attracting application in optical computing, nanodevice formation, and low power. In this paper nanoscale architecture such as the decoder, multiplexer, and comparator are implemented on perpendicular-nano magnetic logic (pNML) technology. All these architectures with the superiority of minimum complexity and minimum delay are pointed. The proposed architectures have been designed using pNML in MagCAD tool, simulated with modelsim platform and correctness shown by simulation waveform. The correctness of these designs can be verified easily when Verilog code is generated from MagCAD tool. The performance of the proposed comparator towards default parameters shows the area of 2.4336 μm2 and critical path of 1.5E-7 sec. As a higher order, the realization of a 4-to-1 multiplexer in NML has also been included in this work.

Keywords: *Comparator; Decoder; Latency; Multiplexer; NML; pNML; QCA.*

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INTRODUCTION

Nano Magnetic Logic (NML) is an emerging technology, which has the ability to replace current CMOS technology because of operating capability in room temperature, high-density integration, low power consumption, non-volatility and absence of, interconnect wires [1]. It has also the facility to integrate logic and memory functionality into the same device, which denotes its great potential for future technology. Perpendicular-nano magnetic logic (pNML) also has the advantages of enabling the fabrication of three-dimensional (3-D) circuits. The fabrication of these 3-D circuits is not cost efficient in conventional CMOS technology because of the presence of vertical interconnections (vias). However, this designing will be very much efficient in pNML technology because of the presence of different layers. To explore this technology simulation tools are needed for designing architectures of nano magnetic logic circuits. Different low-level simulators such as NMAG [2], OOMMF [3] or MUMAX [4] are present for simulating magnetic circuits. But these simulators have limitations in designing small circuits only. Recently researchers have proposed CAD software tool for nano magnetic logic circuits, i.e. Topolinano [5-6] and MagCAD [7]. Both tools can analyse large and complex circuits. In MagCAD tool both in-plane NML (iNML) [8] and perpendicular NML (pNML) [9] circuits can be designed, but in topolinano only iNML circuits are supported. In pNML global and perpendicular clock field is used, which leads to the lower area and power consumption [10]. Different three-dimensional pNML circuits are demonstrated experimentally in [11-13] and memory elements are shown in [14]. The most important feature of pNML is the logic design in-

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memory architecture, which is explained in [15-16]. But till now digital circuits designing using three-dimensional nano magnetic logic circuits are not fully explored. Only exclusive-or gate, half adder, 1-bit full adder, 4-bit ripple carry adder and 32-bit ripple carry adder circuits are designed in [6, 17-21]. The ripple carry adders are designed MagCAD tool by Turvani G *et al.* [6].

In this paper, we further explored digital circuit's architectures using this tool [6]. We designed comparator, decoder and multiplexer circuits using three-dimensional nano magnetic logic circuits. In Section 2, background related to perpendicular-nano magnetic logic circuits are described. In section 3, a new 3-D architecture of 1-bit comparator, 2to4 size decoder, 2to1 and 4to1 size multiplexer's structures are proposed. Finally, in section 4 conclusion is present.

MATERIALS AND METHODS

Quantum-Dot Cellular Automata (QCA) is an emerging technology which has the ability to replace current CMOS technology [22]. It has the beneficial features like higher device density, scalability, higher speed of computation, robust design, lower complexity etc. According to Physical implementation QCA technology is divided to four types (i.e. Metal-island QCA, Semiconductor QCA, Molecular QCA and Magnetic QCA). The sizes of metal-island QCA cell were demonstrated as relatively large in micrometer dimensions. The major disadvantage of this type of QCA is that its operation temperature is extremely low, which is in the range of milli-kelvin [23-24], which prevents the construction of complex QCA circuits running at room temperature. Therefore, this technology is not suitable for future electronics application. A semiconductor QCA cell is composed of four quantum dots manufactured from standard semiconductive materials [25]. In semiconductor QCA, advanced fabrication process is possible similar to existing CMOS processes. However, current manufacturing processes cannot provide mass production for high performance and ultra-small semiconductor QCA devices. To date, most QCA device prototypes only have been demonstrated with semiconductor implementations. In molecular QCA, a basic cell is built upon only molecules. The molecules are expected to be as small as 1 nm or even smaller. Room-temperature operation of a molecular QCA cell has been experimentally confirmed [26]. The difficulty in realizing molecular QCA is due to the high-resolution synthesis methods and positioning of molecule devices. New construction methods for molecular QCA, including self assembly on DNA rafts, are under investigation [27]. However, it is still very difficult to fabricate molecular QCA systems with current technologies.

In magnetic QCA small magnetic dots are present also known as nano-magnets having different functionalities. These nano-magnets can be referred both as a logic element and a memory device, which are made of Co/Pt multilayer for perpendicular NML [28]. Therefore magnetic QCA is called as nano magnetic logic. Although it's operating frequency is low (around 100 MHz), but it has the advantage of room-temperature operation, extremely low power dissipation and high thermal robustness. A simple majority gate using this technology is already fabricated [29]. The first large-scale QCA systems appear to be possible with a magnetic QCA circuit, which has fewer challenges during the manufacturing process compared with other implementations [22]. Because of fabrication advantages, magnetic QCA technology is chosen in this work.

The NML technology is again split up into two types depending upon the magnetic anisotropy. Those are perpendicular NML (pNML) and in-plane NML (iNML). When the magnetic orientation of the nano magnets are in-plane; it is referred as iNML and when the orientation is perpendicular to the plane then it is referred as pNML. Both bistable logic elements logic 0 and logic 1 of iNML and pNML are shown in Fig. 1(a) and 1(b)

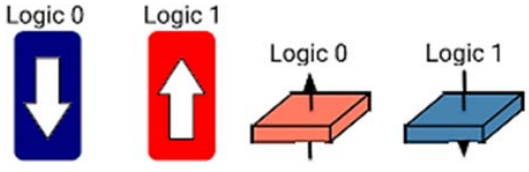


Fig.1 Basic bistable logic elements (a) iNML (b) pNML.

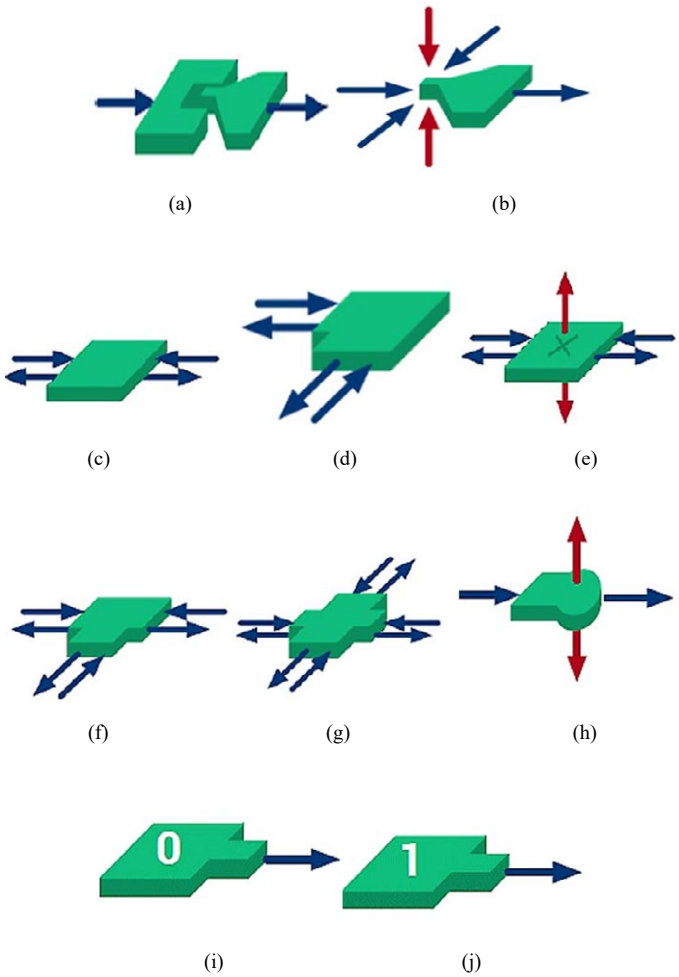
respectively. The direction of Magnetization i.e. whether it is magnetised in one direction or the opposite, commonly referred to as "Up or Down"- is used to represent the binary information. Such as the nano magnet directed in upward direction represents a logic '1' and oriented in downward direction represents a logic '0'.

Both pNML and iNML deal with nano magnets that interact with anti-ferromagnetic behaviour. The iNML has a complex clocking system which is eliminated in pNML [5][7]. Along with it, the pNML has various advantages over iNML such as less power consumption and reduced area occupation. In addition, it also allows the fabrication on three dimensional (3-D) circuits and that too in a cost-effective way as in CMOS technology 3-D circuits comes with a huge fabrication complexity. The pNML circuits start with a nucleation centre and terminate with a pad magnet [7]. This condition should be ensured for proper behaviour of circuit parameters.

Basic Structures of pNML

pNML is the most efficient implementation of the NML technology. In NML, the circuit complexity is reduced due to the use of minority voter (i.e. the minority gate). The minority voter and the inverters are treated as the basic functional units in pNML.

In Fig. 2(a) the pNML structure of an inverter is shown where the input magnet surrounds the output magnet. The output magnet structure [Fig. 2(b)] is called artificial nucleation centre (ANC). Basically, when odd (minimum one and maximum five) numbers of inputs are provided around it, the total structure leads to a minority voter.



(a) (b) (c) (d) (e) (f) (g) (h) (i) (j)

Fig. 2. Basic pNML elements (a) inverter (b) nucleation centre (c) domain wall magnet (d) corner magnet (e) Via magnet (f) T-connection (g) X-connection (h) Pad magnet (i) Fixed '0'Magnet (j) Fixed '1' magnet.

Similarly, there are various magnetic elements in pNML performing several functions. The structure shown in Fig. 2(c) is a normal magnet (also known as domain wall) which is the basic element of this promising technology. It is mainly used to route signals. The Fig. 2(d) shows the structure of a corner magnet which is also a normal magnet but with 90^0 rotation. In Fig. 2(e), there is a via magnet which is used to connect to a nucleation centre situated on another plane. So by use of this, we can have one or two inter-layer outputs.

The T-connection magnet shown in Fig. 2(f) is used to split the input into two different directions. The cross-connection magnet shown in Fig. 2(g) is also a simple magnet that splits the input in three different directions. The Fig. 2(h) shows a pad magnet which is mainly used as the termination of a magnetic wire. Only a nucleation centre can be used as its output. To implement different functions in pNML we need to provide certainly fixed inputs. The structures shown in Fig. 2(i) and Fig. 2(j) are the fixed '0' and fixed '1' input magnets respectively.

A minority voter is shown in Fig. 3. Here there are three numbers of inputs namely A, B and C. All these inputs are connected to nucleation centres, nucleation centres are connected to domain walls, domain walls are connected to corner magnets and corner magnets are connected to pad-magnets. Here A, B and O outputs are in the same layer, whereas C input is in a different layer. The output expression is

$$Y = M(A, B, C) = \bar{A}\,\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}. \quad (1)$$

Unlike molecular QCA, if any of its inputs are fixed to 0 then it gives the NAND logic output and if the input is fixed to 1 then it behaves as a NOR gate. In the minority voter, it is necessary to have equal geometry and distance of the three inputs to the nucleation centre of the output for the proper operation of the gate. In pNML for proper propagation of the information within the circuit a perpendicular clock field is applied and after every clock cycle, the output of each building block is placed in anti-parallel compared to the previous input [27]. Because of this reversal mechanism, the output of every building block can be used as input for next block. So signal propagation takes place in a step by step manner according to the clocking field.

RESULTS AND DISCUSSIONS

The proposed works are based on pNML technology. In pNML all the layout designs start with a nucleation centre i.e. the initial input is given to the nucleation centre. Here a 1-bit comparator, a 2to4 decoder, a 2to1 multiplexer (MUX) and a

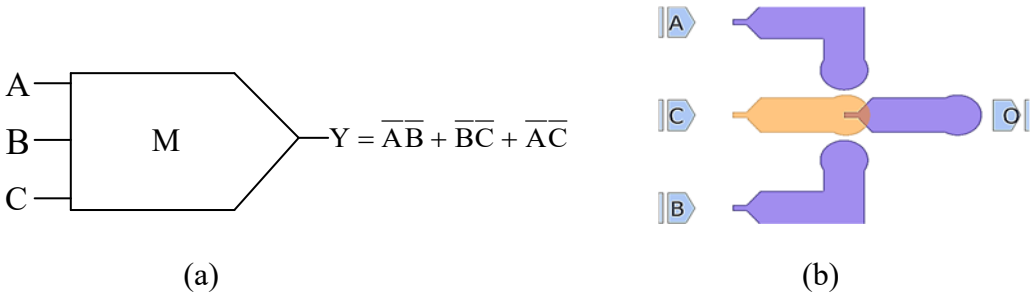


Fig. 3. Minority voter (a) block diagram (b) 3-D Minority Voter.

Table 1. Geometrical and Physical parameters.

Parameters	Value
Nanowire width	40nm
Grid size	120nm
Inter magnet space	150nm
Co thickness (Co=Cobalt)	3.2 nm
stack thickness	6.2nm
volume of ANC	$1.68 \times 10^{-23} m^3$
Clock field amplitude	560 Oe
Inverter coupling field strength	153Oe
Minority gate coupling field strength	48 Oe
Effective anisotropy	2.0×10^5 J/m^3

4to1 multiplexer circuit's layouts using pNML concept is proposed. All the layouts are designed using MagCAD tool [7]. After the formation of layouts, VHDL netlist will be extracted. This netlist file is the replication of the circuit behaviour, which functionality is tested using ModelSim simulator, with providing proper test bench. Geometrical and physical parameters are provided in Table 1.

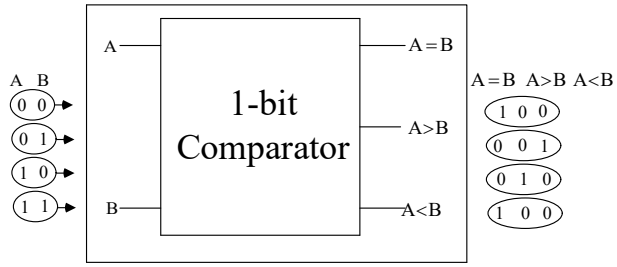
Comparator Design in pNML

The comparator is a digital electronic circuit that compares two numbers. Here in this work the layout of a 1-bit comparator using the pNML technology has been proposed. In this circuit there are two 1-bit inputs i.e. A and B and it produces three outputs (1-bit) such as P for input A is less than input B (A<B), Q for A equals to B (A=B) and R for A is greater than B (A>B) which is shown in Fig. 4(a).

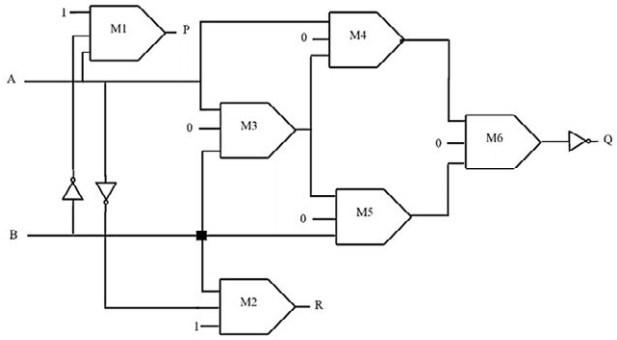
The minority gate schematic diagram is shown in Fig. 4(b) and pNML layout is illustrated in Fig. 4(c). The expressions for comparator outputs are derived in below equations using minority voters.

$$P = M1(1, \bar{B}, A) = 0 + B\bar{A} + 0 = \bar{A}B \tag{2}$$

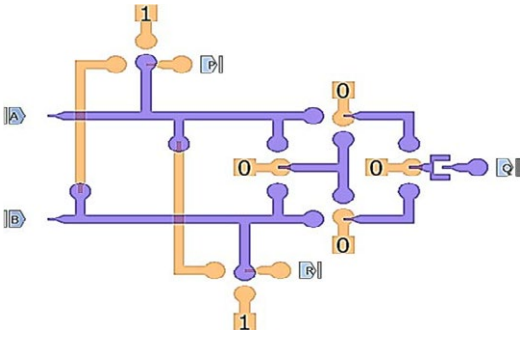
$$\begin{aligned} Q &= \overline{M6\,(\,M4(A, 0, M3\,(A, 0, B)), 0, M5\,(M3\,(A, 0, B), 0, B))} \\ &= \overline{(M6\,(\,M4(A, 0, \overline{AB}), 0, M5\,(\,\overline{AB}, 0, B))} \\ &= \overline{M6\,(\,\overline{A.\overline{AB}}, 0, \overline{\overline{AB}.B})} \\ &= \bar{A}\bar{B} + AB \end{aligned} \tag{3}$$



(a)



(b)



(c)

Fig. 4. 1-bit comparator (a) block diagram (b) schematic (c) 3-D pNML layout.

$$\mathrm{R} = M2\,(B, \bar{A}, 1) = \bar{B}A + 0 + 0 = A\bar{B} \quad (4)$$

The proposed design is a 3-D circuit because the magnetic wires are in different layers. According to the nano-magnetic phenomenon an input in a particular layer is propagated in its inverted form in another layer i.e. we can get the invert of an input by just changing the layer.

Here both the inputs A and B are given to the circuit layer '0' initially. To get the P output, the input A is applied to the minority voter directly in layer '0' but the input B is applied in layer '1' so as to provide its inverted form without using an inverter circuit. Then a fixed '1' input is given to the other input terminal of the minority voter. The basic concept of perpendicular-nano magnetic logic states is that if any of the inputs of a minority voter is being logic '0' then it will function as a NOR gate. Hence the minority voter produces the required output P. Similarly to get the R output, the input A is applied in the same layer '0' to the minority voter but input B is applied in layer '1' to get the inverted B. Here also a fixed '1' input is given to the minority voter and then it produces the output R which is high when input A is greater than input B. To get the output Q, it requires four numbers of minority voters along with an inverter which in term forms an Ex-NOR gate.

The above Fig. 5 shows the simulation result of the proposed layout of the 1-bit comparator. The result clearly shows that the proposed design successfully satisfies the truth table of the 1-bit comparator. The total design occupies a bounding box area of 2.4336 μm^2 and it uses only six numbers of minority voters and one inverter in the total circuit. The circuit shows a critical path delay of 0.15μs. It also exhibits different latencies for different input combinations which are tabulated below.

Decoder Design in pNML

Decoders are also called as function selector, which converts n number of inputs to 2^n numbers of outputs. So its standard size is n×2^n. Here a 2×4 decoder design is proposed, which is implemented using the pNML concept. The block diagram is shown in Fig. 6(a). The Fig. 6(b) and Fig. 6(c) shows the minority gate schematic and proposed pNML layout of the 2:4 decoder respectively. It is an active high output decoder, i.e. only one output bit is high at a time. In the pNML layout, four numbers of minority voters and inverters are used. Here A and B are the inputs to the decoder circuit. In the layout of all minority voters fixed 0 inputs are used which are behaving as NAND logic gates where outputs are D_0=A'B', D_1=A'B, D_2=AB' and D_3=AB.

The boolean expressions for the decoder outputs (Fig. 6(b)) using minority gates are shown in below equations

$$D0 = \overline{M1(\bar{A}, \bar{B}, 0)} = \overline{\bar{A}\,\bar{B}} = \bar{A}\,\bar{B} \quad (5)$$

$$D1 = \overline{M4(M2(A, 0, B), B, 0)}$$

$$= \overline{M4\,(\overline{AB}\,, B, 0)} = \overline{\overline{AB}.B} = \overline{AB}\,.B = \bar{A}B \quad (6)$$

$$D2 = \overline{M3\big(0, A, M2(A, 0, B)\big)}$$

$$= \overline{M3\,(0, A, \overline{AB})} = \overline{\overline{AB}.A} = \overline{AB}\,.A = A\bar{B} \quad (7)$$

$$D3 = \overline{M2(A, 0, B)} = \overline{\overline{AB}} = AB \quad (8)$$

The layout occupies a bounding box area of 1.0368μm^2. It has a critical path delay of 0.142μs.

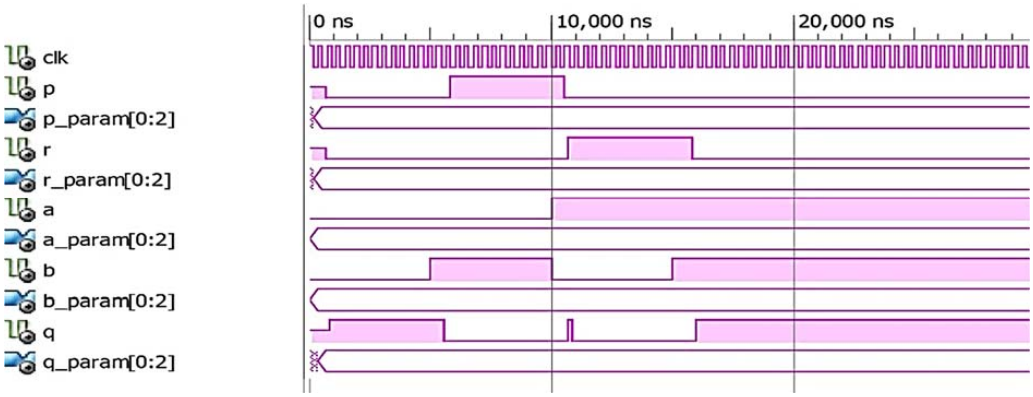


Fig. 5. Simulation Result of the pNML layout of 1-bit Comparator.

The Fig. 7 shows the simulation result of the proposed 2to4 decoder. Here there is a latency of 870 ns for D_0, 1620 ns for D_1, 860 ns for D_2 and 850 ns for D_3 outputs. The Table 3 below shows all the features of the proposed design along with the delays for several input combinations.

Multiplexers Design in pNML

The multiplexer is a universal circuit, which is also known as Data Selector, Many to One, and Parallel to Serial Converter. Here a 2to1 MUX has been implemented using the perpendicular-nano magnetic logic. The block diagram and minority-gates schematic diagram are shown in Fig. 8(a) and 8(b) respectively. The pNML layout of the proposed MUX having two input lines namely I_0 and I_1, are applied to the circuit through the nucleation centres. This is illustrated in Fig. 8(c). The 2to1 MUX design proposed in this paper comprises only three numbers of minority voters without any inverter circuit.

In pNML, logic '0' in a particular layer behaves as logic '1' in another layer. This property of pNML has been exploited to design the proposed layout of the MUX circuit. The selection input S is provided to the initial two minority gates in two different layers. Hence one of the two minority voters is getting a direct input S and the other is getting its inverted one i.e. S'.

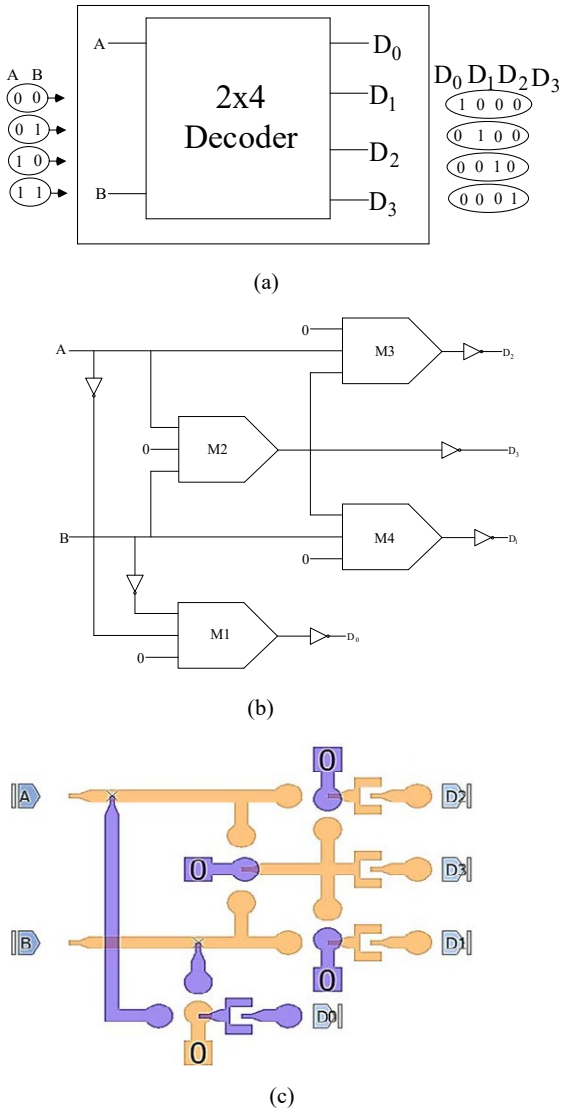


Fig. 6. Decoder of 2-to-4 size (a) block diagram (b) pNML schematic (c) 3-D pNML layout.

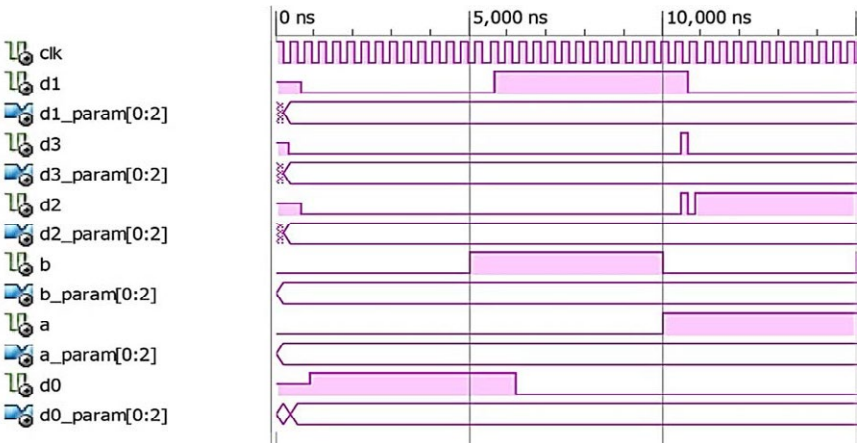
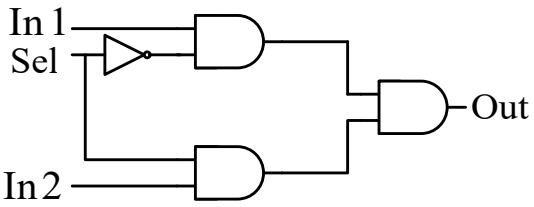
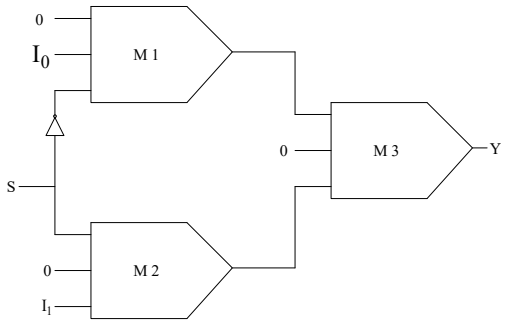


Fig. 7. Simulation Result of Proposed Layout of 2:4 Decoder.



(a)



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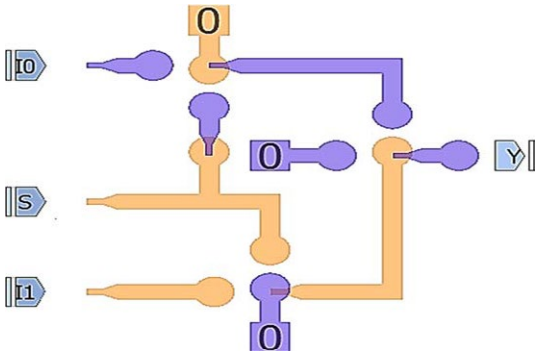

(c)

Fig. 8. multiplexer of 2:1 size (a)block diagram (b)pNML schematic (c) 3-D pNML layout.

This design is based on NAND realization of 2to1 MUX. All the three minority voters in the layout are having a fixed '0' input along with other two inputs; so that these minority voters behave as NAND gates. Hence the circuit finally produces an output as $Y=I_0S+I_1\bar{S}$. The inputs are applied in different layers rather than using any additional inverting circuit which reduces the complexity of the proposed circuit layout. The Boolean expression for 2to1 MUX using minority gates is given below.

$$Y = M3\big(M1(0, I0, \bar{S}), 0, M2(S, 0, I1)\big)$$
$$= M3\big(\overline{\bar{S}\,.\,I0}, 0, \overline{S.I1}\big) \quad (9)$$
$$= \overline{\overline{\bar{S}.I0}\,.\,\overline{S.I1}} = \overline{\overline{\bar{S}.I0}} + \overline{\overline{S.I1}} = \bar{S}.I0 + S.I1$$

This design occupies a bounding box area of 0.8056μm^2. It exhibits a critical path delay of 0.14μs. The simulation result of the proposed layout of 2to1 MUX is shown in Fig. 9 below. Here from the waveform, it is shown that when the selection line S is being 0, the circuit output Y is equal to I_0 value and when S is equal to 1, then the circuit output will be I_1 value. Here I_0 is set as logic '1' and I_1 is set to logic '0'. For S=0 we are getting Y=1 with a latency of 855 ns and for S=1, we are getting Y=0 with a delay of 1000 ns. The same has been tabulated below in Table 4.

In this paper, a novel 4to1 size multiplexer pNML layout is also proposed which is formed by the proper connection of three numbers of 2to1 multiplexers proposed earlier in this work. As each 2to1 MUX consists of three numbers of minority voters, so a total of nine number of minority voters are used to design the whole 4to1 MUX circuit.

The block diagram and pNML layout are illustrated in Fig. 10 (a) and (b) respectively. This design is also free from inverters. Here there are four input lines i.e. I_0, I_1, I_2 and I_3 along with two numbers of selection lines S_0 and S_1. All the inputs except I_0, are in layer '1' and I_0 is in layer '0'. The layers of the inputs are changed in some cases before applying it to the minority voters in order to get its inverted form as per our requirement.

Fig. 11 shows the simulation result of the proposed layout of 4to1 MUX. From this result, we can conclude that the proposed layout completely satisfies the truth table of 4to1 MUX. The proposed circuit produces the expected output with some delay which has been tabulated below in Table 5.

Here the input values are set as I_0=1, I_1=0, I_2=1 and I_3=0. From the simulation result it can be seen that when the selection inputs S_0 and S_1 are being 0, the circuit produces the output Y as 1 (as I_0=1) with a latency of 1144 ns. Similarly, for S_1=0 and S_0=1, we are getting Y=0 with a latency of 1132ns, for S_1=1 and S_0=0, the circuit is producing the output Y=1 and for S_1=1 and S_0=1, Y is being 0 with a latency of 1535ns. The total design occupies a bounding box area of 2.9376μm^2 and exhibits a critical path delay of 0.159 μs. The below Table 6 shows the comparison of the proposed NML circuits with the existing CMOS technology. The comparative performance results in Table 6, also proven that the nano-magnetic based implementation of the comparator, decoder and multiplexer has efficient

Table 2. Performance table of 1-bit Comparator.

3-D Comparator (1-Bit) Bounding Box Area = 2.4336 μm^2 Critical path= 1.5E^{-7} sec					
Inputs		Outputs			Latency
A	B	P	Q	R	(in sec)
0	0	0	1	0	0.88E^{-6}
0	1	1	0	0	0.79E^{-6}
1	0	0	0	1	0.89E^{-6}
1	1	0	1	0	0.99E^{-6}

Table 3. Performance table Proposed of 2:4 Decoder.

3-D Decoder(2:4) Bounding Box Area= 1.0368μm^2 Critical Path=1.42E^{-7}						
Inputs		Outputs				Latency
A	B	D_0	D_1	D_2	D_3	(in sec)
0	0	1	0	0	0	0.87E^{-6}
0	1	0	1	0	0	1.62E^{-6}
1	0	0	0	1	0	0.86E^{-6}
1	1	0	0	0	1	0.85E^{-6}

Table 4. Performance Analysis of Proposed 3-D 2×1 MUX.

3-D 2×1 MUX Critical Path=1.4E^{-7}s Bounding Box Area=0.8064μm^2		
Input pattern	Output pattern	Latency
S	Y	(in sec)
0	I_0	0.85E^{-6}
1	I_1	0E^{-6}

Table 5. Performance Analysis of Proposed 3-D 4×1 Multiplexer.

3-D 4×1 MULTIPLEXER Bounding Box Area= 2.9376μm^2 Critical Path= 1.5E^{-7}sec			
Inputs		Output	Latency
S_1	S_0	Y	(in sec)
0	0	I_0(=1)	1.1E^{-6}
0	1	I_1(=0)	1.1E^{-6}
1	0	I_2(=1)	1.5E^{-6}
1	1	I_3(=0)	1.5E^{-6}

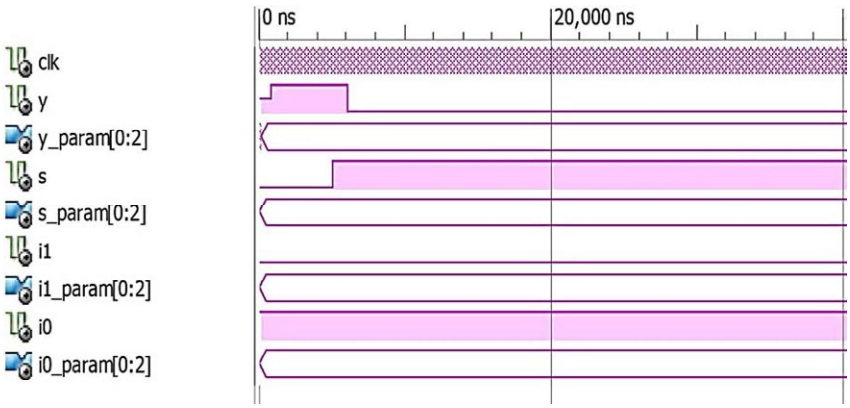

Fig. 9. Simulation Result of the Proposed 2×1 MUX Layout.

Table 6. Comparison with existing CMOS technology.

	Exiting CMOS 45nm Technology in (Area)	Proposed pNML (Area)
1-bit Comparator	58.80 μm^2 [30]	2.43 μm^2
2:4 Decoder	22.4 μm^2 [31]	1.03 μm^2
2:1 Multiplexer	28.9 μm^2 [32]	0.80 μm^2

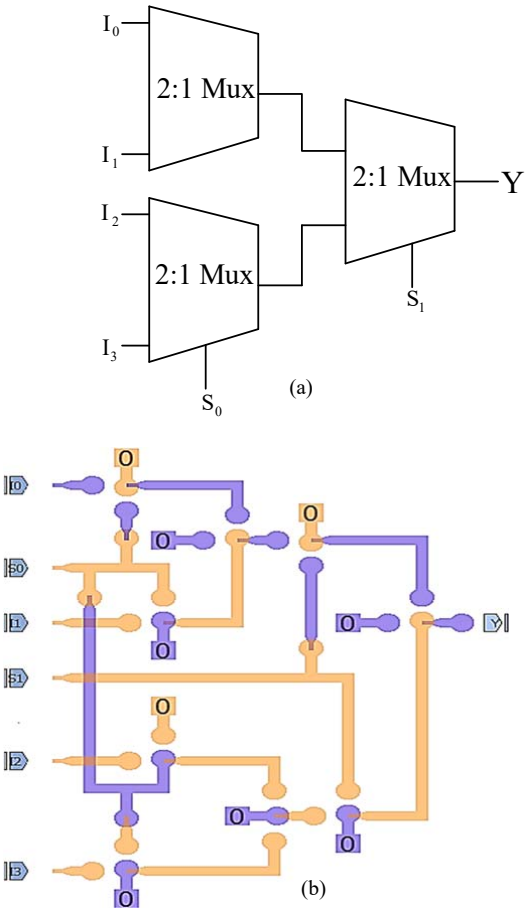

Fig. 10. Multiplexer of 4:1 size (a)Block Diagram (b) 3-D pNML Layout.

results in all the primitives as compared to the existing CMOS implementation.

CONCLUSION

In the article, we have designed nano-magnetic based computing in emerging devices as a promising domain for high speed and high-density integration. A new synthesis of implementing magnetic dipole based comparator, decoder and multiplexer are presented. These proposed architectures produce less latency which is easily verified by performance analysis tables. The latency results depict that the fast synchronization of inputs and outputs and shows an efficient implementation in the physical foreground. All the layouts proposed in this paper are implemented on the MagCAD tool using pNML technology. We have shown that the nano magnetic logic offers superior results with miniaturization of the area for proposed designs as compared to existing 45nm CMOS technology. The grid size and magnet width of all the magnetic elements are set as 120nm and 40nm respectively. MagCAD tool generates VHDL file for the designed layout and to test the functionality of the newly designed circuits. This file functionality is later verified in the ModelSim software. The miniaturisation of area properties of the nano-magnetic based present designs has afforded avenues for the miniaturizations and implementation of future electronics applications.

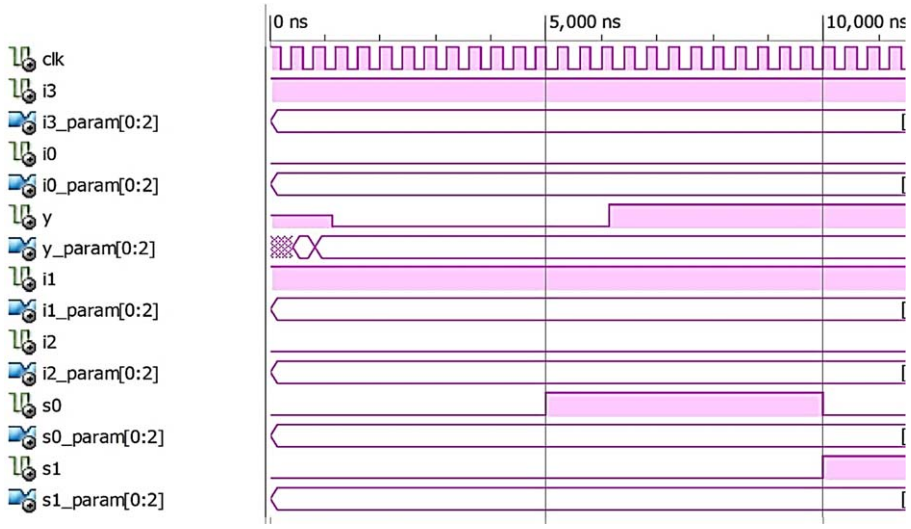

Fig. 11. Simulation result of the 3-D pNML Layout of 4×1 Multiplexer.

CONFLICT OF INTEREST

The authors declare that there are no conflicts of interest regarding the publication of this manuscript.

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