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High-Speed Penternary Inverter Gate Using GNRFET

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Abstract

This paper introduces a new design of penternary inverter gate based on graphene nanoribbon field effect transistor (GNRFET). The penternary logic is one of Multiple-valued logic (MVL) circuits which are the best substitute for binary logic because of its low power-delay product (PDP) resulting from reduced complexity of interconnects and chip area. GNRFET is preferred over Si-MOSFET for circuit design due to its fantastic thermal, mechanical and electrical properties. For this circuit design, the voltage divisions obtained with resistors. All the circuits are simulated and compared by HSPICE, 15nm GNR Technology with the supply voltage of 0.8V. Simulation results demonstrate that the PDP is about 1e-18. Therefore, MVL design based on GNRFET leads to minimum PDP than other devices such as CNTFET. Furthermore, the transient wave is absolutely accurate. The variation of the figure of merits (FOM) such as power consumption, propagation delay, and PDP is investigated as a function of a number of the ribbon in GNRFET structure.

Keywords: *GNRFET, Penternary Logic, Power-Delay Product, Inverter*

1. Introduction

MVL circuit design is noteworthy for circuit designer due to advantages over binary logic. Since each wire can transmit more data than binary logic, the number of interconnections to execute functions is reduced and the complexity of the chip is decreased [1]. Hence, the MVL circuit design provides low power dissipation. Multiple-Valued logic circuits are designed in current-mode and voltage-mode [2-4]. The transistors with a different threshold voltage are required for designing the MVL voltage-mode circuit. In GNRFET circuit designs, by changing width will be the different threshold voltage.

Graphene is the first synthetic two-dimensional (2D) atomic crystal. Graphene is an ideal material for the MVL design because the conductivity of graphene is linearly proportional to the gate bias [5]. Graphene is a 2D zero band gap semimetal. Therefore, its band gap must be opened up before it can replace CNTFET and be used in electronics. One way is to convert graphene to nanoribbon shape. The edge of graphene can be classified as either armchair or zigzag. The zigzag edge GNRs show metal properties, whereas the armchair edge GNRs can be of either metal or semiconductor [6].

In the previous works, there are many techniques which are demonstrated for implementing MVL circuits, based on CNTFETs [2, 7-13]. Ternary logic designs with

resistors have been proposed in [2]. Lin *et al* design the ternary logic circuit with transistor [7]. Fakhari *et al* design the quaternary logic circuit with pass transistor logic [8]. The universal method presented in [9] for design MVL circuit based on CNTFET. Three input ternary logic circuit and two input quaternary and penternary are simulated in [10]. Robust Carbon Nanotube Field Effect Transistor-Based Penternary Logic Circuits is considered in [11]. They have applied a buffer to design with four different CNT diameters. In the rest of the paper, the structure of Graphene nanoribbon field effect transistor is described in section II. In Section III, the proposed work is introduced and described. Afterward, the performance analysis results are presented before the conclusion section.

2. Graphene Nanoribbon Field Effect Transistor

Graphene is two-dimensional (2D) atomic crystal. Lately, some graphene transistor structures have been investigated such as back-gated graphene transistors, dual-gate graphene transistors, and graphene nanoribbon FETs [14-16]. The electronic and physical characteristic of graphene nanoribbons (GNRs) can be managed by changing their width and edge structure. Recent experimental results have illustrated the bottom-up chemical synthesis of ultra-narrow GNRs with uniform width and edges. This GNRs with high structural and electronic that is required for the integration of GNR field-effect transistors (FETs) into ultra-large-scale digital circuits [17].

The armchair edge GNRs (AGNRs) of the type N = 3P+1 and N=3P are semiconductor while AGNR of type N=3P+2 is metallic where P is a positive integer [18]. This type of GNR is used for digital circuit design. The width of a GNR is defined as follows [19]:

$$W_{ch} = (N+1)\sqrt{3} \times \frac{dcc}{2} \qquad (1)$$

Where N shows the number of dimmer lines and dcc= 0.144 nm is the carbon-carbon bond length. The channel of our devices is composed of four parallels nanoribbon is shown in Fig1.

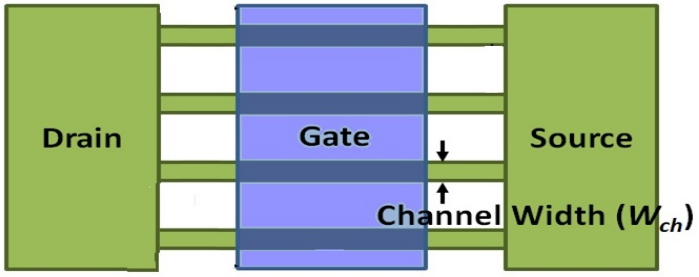


Figure1. The structure of the four-ribbons GNRFET.

3. Proposed Design

In MVL systems permit more than two logic levels. Ternary logic includes 0, $1/2V_{DD}$, V_{DD} voltage levels. The quaternary logic level contains 0, 1/3 V_{DD}, 2/3 V_{DD}, V_{DD} voltage levels. Penternary logic level can be demonstrated with '0', '1', '2', '3' and '4'

symbols, which are equivalent to 0, 1/4 V_{DD} , 2/4 V_{DD} , 3/4 V_{DD} , V_{DD} . The truth table of penternary inverter is given in Table 1.

Table 1. Truth table of penternary inverter

Input	Out put
0	V_{DD}
1/4 V_{DD}	3/4 V_{DD}
1/2 V_{DD}	1/2 V_{DD}
3/4 V_{DD}	1/4 V_{DD}
V_{DD}	0

To achieve the precise voltage logic level is applied the resistors. The threshold voltage of GNRFET changes with its width. The parameters of the GNRFET model [20], their values, and brief descriptions are given in Table 2.

Table 2. The important HSPICE parameters of the GNRFET

Device parameter	Description	Default value
L	Physical channel length	15nm
Tox	The thickness of top gate dielectric material (planer gate)	0.95nm
2Wsp	The spacing between the edges of two adjacent GNRs within the same device	2 nm
NRib	The number of GNRs in the device	4
P	The edge roughness percentage of the device	0
Dop	Source and drain reservoirs doping fraction	0.001
Tox2	Oxide thickness between channel and substrate/bottom gate	20nm
Gates_tied	Whether Gate or sub hold the same voltage	0

The first proposed penternary inverter design based on GNRFET is shown in Fig 2a. The transient responses of the proposed design are demonstrated in Fig 2b. The widths of T1, T2, T3, T4, and T5 are 0.99 nm, 1.2 nm, 1.9, 2.3 nm, 2.3 nm respectively. The width of GNRFET has Inverse relationship with the threshold voltage.

The power supply voltage is 0.8V. When the input is 0V, all n-type are off and p-type is on. Hence, the V_{out} is V_{DD}. By increasing the input to 1/4 V_{DD}, T2 and T5 get on and the output is as follow:

$$V_{out} = \frac{10k\Omega}{(10+30)k\Omega} V_{DD} = \frac{1}{4} V_{DD} \quad (1)$$

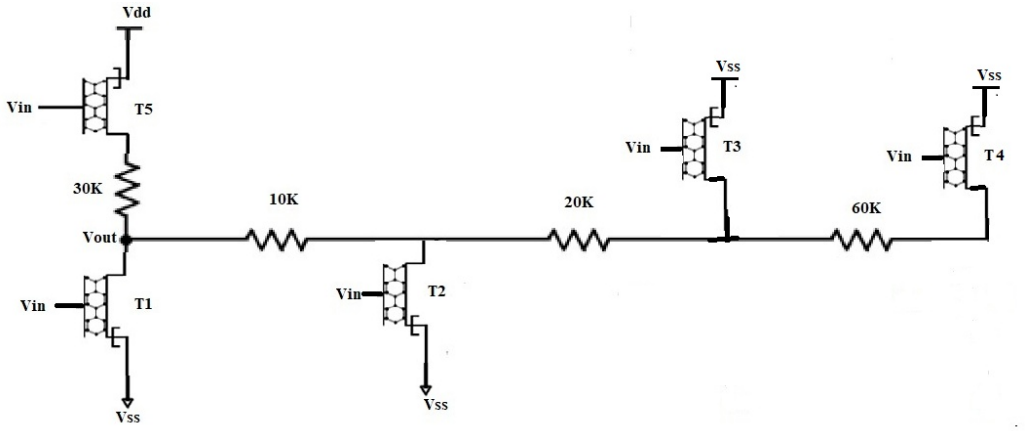
When the input reaches to 1/2 V_{DD}, T3 and T5 are on and the V_{out} obtained as follow:

$$V_{out} = \frac{(10+20)k\Omega}{(10+20+30)k\Omega} V_{DD} = \frac{1}{2} V_{DD} \quad (2)$$

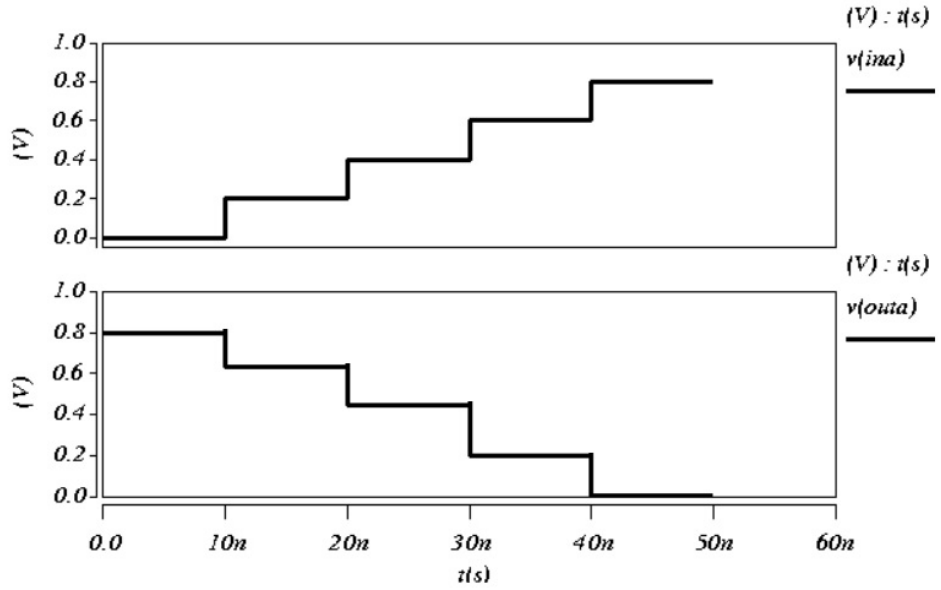
When the input accrues to 3/4 V_{DD}, T4 and T5 are on and the output voltage is:

$$V_{out} = \frac{(10+20+60)k\Omega}{(10+20+60+30)k\Omega} V_{DD} = \frac{3}{4} V_{DD} \quad (3)$$

Finally, when the input is V_{DD}, only T1 is on and the output is 0V.



a)



b)

Figure2. a) Proposed penternary inverter design based on GNRFET.
b) Transient response of penternary inverter.

Simulation results of the figure of merit are given in Table III. Results show that digital circuit design based on GNRFET has significantly less PDP than CNTFET.

Table 3. Simulation results of the penternary inverter

Design	Power (e-6w)	Delay (e-12s)	PDP (e-18J)	Number of transistors
proposed design	3.77	0.333	1.255	5
Ref [21]	3.92	22.688	88.99	5
Ref [11]	3.41	7.85	267.685	14
Ref [10]	1.9560	65.126	127.3864	12

4. Performance Analysis

For the evaluation of proposed design, we investigated the power, delay and product delay- power as the figure of merit with the different number of ribbon. As depicted in Fig 3, power increases by increasing the nribbon.

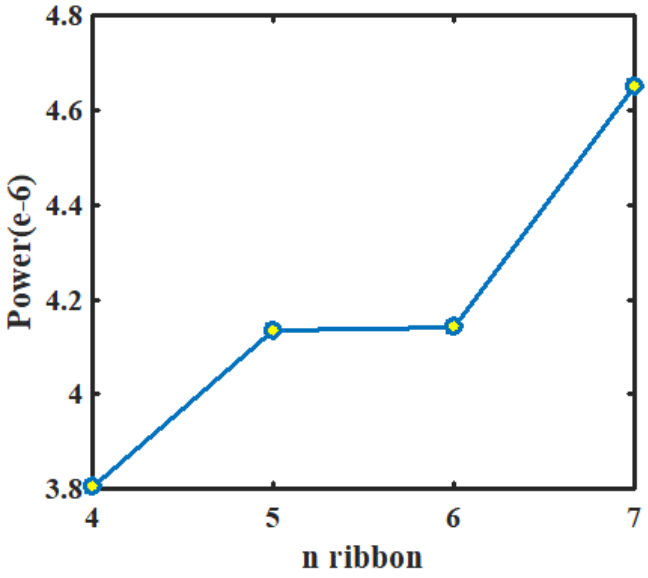


Figure3. Power as function of nribbon

Furthermore, by increasing the number of ribbon in GNRFET structure, delay increase.

Fig4 illustrates the variation of delay versus of nribbon.

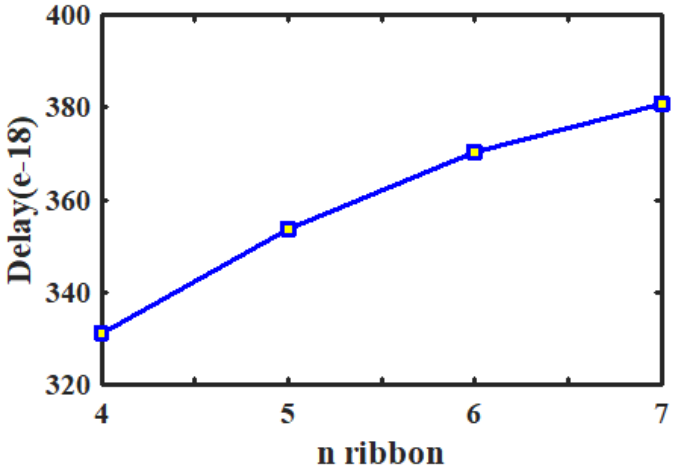


Figure4. Delay as function of nribbon

Fig5 shows the variation of PDP as the function of nribbons. PDP increases by increasing the number of ribbons.

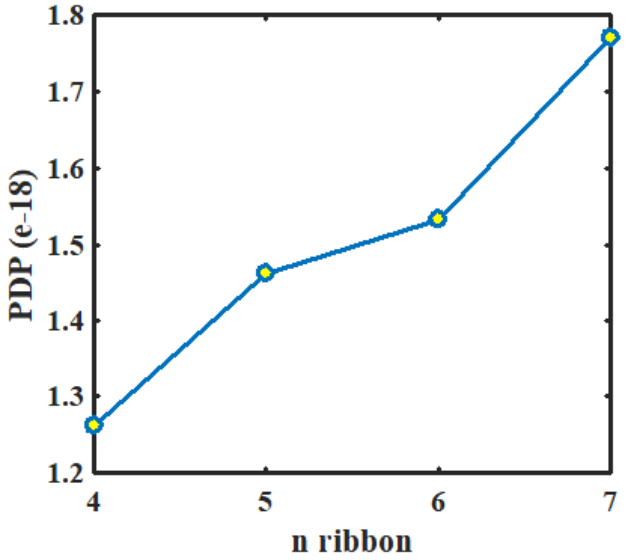


Figure5. PDP as function of n ribbon

5. Conclusion

GNRFET with the superior electronic properties is a good candidate for next-generation of the integrated circuit. GNRFET has the thinnest channel with 15-nm. MVL circuit has less area and computation step than binary. In this paper, we proposed the inverter penternary gate based on GNRFETs for the first time. Results show that the proposed work is ultra-high-speed. Furthermore, the PDP of GNRFET is less than CNTFET in the literature. Hence, GNRFET can be used for the digital circuit design.

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