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ORIGINAL ARTICLE

High speed Radix-4 Booth scheme in CNTFET technology for high performance parallel multipliers

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Abstract

A novel and robust scheme for radix-4 Booth scheme implemented in Carbon Nanotube Field-Effect Transistor (CNTFET) technology has been presented in this paper. The main advantage of the proposed scheme is its improved speed perfor-mance compared with previous designs. With the help of modifications applied to the encoder section using Pass Transistor Logic (PTL), the corresponding capacitances of middle stages have been reduced considerably. As a result, total transistor count along with power consumption has been decreased illustrating the other advantages of the designed structure. For evaluation of correct functionality, simulations using CNTFET 32nm standard process have been performed for the de-signed scheme which depict the latency of 195ps for critical path. Meanwhile, comparison with previous works using the Power Delay Product (PDP) criteria demonstrates the superiority of the proposed structure suggesting that our circuitry can be widely utilized for high speed parallel multiplier design.

Keywords: *CNTFET; High Speed; Low Power; Parallel Multiplier; Radix-4 Booth Scheme.*

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INTRODUCTION

Having the diameter size in the scale of nanometer which can change up to a few micrometers in length, Carbon Nanotubes (CNTs) contain one-dimensional tubular structure [1], which are introduced first by Iijima in 1991 [2]. In this presented model, thick graphene sheet has been used to define the CNT and based on the number of layers; different categories of CNTs can be specified [3]. For consumer electronics, Single-Wall CNTs (SWCNTs) showed good promise to manufacture the next generation of Integrated Circuits (ICs) because of their unique structural properties [4]. However, the first reliable implementation of CNT Field-Effect Transistor (CNTFET) circuits is achieved about 15 years after Iijima's invention [5].

A brief review of state-of-the-art works in the field of CNTFETs demonstrate that wide range of electronic devices involving low power digital electronics [6, 7] are nowadays being fabricated using CNTs to benefit from the low power and high speed characteristics of the CNTFET devices. The CNTFET device can be utilized in the implementation of the high performance microprocessors, too. One of the basic building blocks of modern microprocessors is the parallel multiplier which lies in the critical path for delay of the block and directly determines the power and speed performance of such systems [8].

Because of their higher performance, parallel multipliers are the design choice for circuit designers [9], although their building blocks are more complicated than their serial counterparts [10]. Among the different procedures utilized for implementation of a parallel multiplier, radix-4 Booth algorithm is one of the popular structures due to its unique capability for reduction of

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the Partial Products (PPs) at the first stage of multiplication process [8]. Knowing that a general purpose parallel multiplier has been composed of three main stages [11], including Partial Product Generation (PPG) block, Partial Product Reduction Tree (PPRT), and the final adder stage, the circuitry pertaining to Booth algorithm constitutes the first stage of multiplication chain in which the PPs are determined by means of this procedure.

Although there are several works for hardware realization of Booth algorithm in the literature [12-18], all of them have been designed in Complementary Metal-Oxide-Semiconductor (CMOS) submicron technologies. Among these works, comparative analysis shows that in [13-15] the operation speed was targeted as the main factor while the power optimization was the primary emphasis in [12, 16-18], both parameters were the subject of improvement where the cost paid was a complicated error-tolerant system.

The main idea behind this article is based on a previous work by the authors [19] in which a novel low power scheme was presented for implementation of the second stage of a parallel multiplier consisting of 4-2 compressors. Following that work, in this paper, a robust scheme has been presented for radix-4 Booth algorithm in CNTFET technology, which depicts better specifications in comparison with the previous designs. In order to demonstrate the advantage of the proposed structure, the best reported works in literature have been redesigned and simulated here in CNTFET technology for fair comparison.

The organization of manuscript is as follows. In section 2 of the paper, the design of the proposed architecture has been discussed, while the simulation results and comparative analysis were explained in section 3. The conclusions will be given in section 4 of the paper.

EXPERIMENTALS

Along with the introduction of the term *Parallel Multiplier* by Arthur Robinson [20], the middle years of the 20th century has faced an evolution of different procedures for fast multiplication including Booth [21], Karatsuba [22], Wallace [23] and Dadda [24] algorithms. Among these methods, Booth algorithm has attracted the attention of circuit designers over recent years because of its exciting properties for effective coding of binary numbers, which could lead to the reduction of PPs in a multiplier array.

By defining *A* as the first number known as multiplicand and *B* as the second number denoted as multiplier [20], the binary representation of these numbers can be expressed as:

$$\begin{cases} A = a_{n-1}a_{n-2}\ldots a_1a_0 \\ B = b_{n-1}b_{n-2}\ldots b_1b_0 \end{cases} \quad (1)$$

where a_i and b_i illustrate each bit in binary basis. With the help of Booth algorithm and by decomposing *B* to its adjacent pair of bits, the multiplication of *A* and B can be written in the form of:

$$A \times B = A \times \left(-b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i\, 2^i \right) \quad (2)$$

in which $b_{-1} = 0$ and n represent the maximum number of bits for both numbers. Equation (2) is well known as radix-2 Booth multiplication routine, which can multiply two signed binary numbers. By modifying B as is presented in [14] and rewritten herein Eq. (3):

$$B = \sum_{i=0}^{\frac{n}{2}-1} (b_{2i-1} + b_{2i} - 2b_{2i+1})2^{2i} \quad (3)$$

and defining:

$$d_i = b_{2i-1} + b_{2i} - 2b_{2i+1} \quad (4)$$

as the radix-4 sign digit representation coefficient, the substitution of (3) and (4) in (2) results in:

$$A \times B = \sum_{i=0}^{\frac{n}{2}-1} A \times d_i\, 4^i \quad (5)$$

Now, comparison of (2) and (5) demonstrates that employing such coding which is known as radix-4 Booth algorithm, the number of PPs (defined by *n*) are almost halved. Therefore, huge speed enhancement is expected if this method is utilized for the hardware implementation of a parallel multiplier. Meanwhile, the coefficient d_i in Eq. (5) is an indication of scale factors (-2X, -X, 0, X, 2X) for multiplication process. Table 1 summarizes the conventional truth table used for radix-4 Booth scheme implementation.

The architectures reported in [12-13] have utilized the conventional truth table for implementation of their circuits. However, none of them could reach latencies less than 4 XOR logic

Table 1. Conventional Truth Table for Radix-4 Booth Scheme.

d_i	b_{2i+1}	b_{2i}	b_{2i-1}	X	$2X$
0	0	0	0	0	0
1	0	0	1	1	0
1	0	1	0	1	0
2	0	1	1	0	1
-2	1	0	0	0	1
-1	1	0	1	1	0
-1	1	1	0	1	0
-0	1	1	1	0	0

Table 2. Proposed Truth Table Of Booth Scheme From [14].

d_i	b_{2i+1}	b_{2i}	b_{2i-1}	Neg	X	Z
0	0	0	0	0	0	0
1	0	0	1	0	1	1
1	0	1	0	0	1	1
2	0	1	1	0	0	1
-2	1	0	0	1	0	1
-1	1	0	1	1	1	1
-1	1	1	0	1	1	1
-0	1	1	1	1	0	0

gates. On the other hand, the structures in [14-15] have introduced new truth tables which were the extended version of the general truth table. The result of this modification was the achievement of 2 XOR logic gate level delays from inputs to the outputs.

The main novelty of the design proposed in [14-15] was the elimination of *2X* scale factor inside the encoding stage. They instead introduced one or two new intermediate parameters which led to the implementation of high speed architecture. One of the common parameters among all previously presented works is the sign bit factor which is denoted as *Neg*. An in-depth view of the proposed ideas depicts that simpler structures can be obtained for the radix-4 Booth encoding-decoding scheme. Considering Table 2 which was previously reported in [14], it is clear that the parameter $\bar{Z}$ equals to:

$$\bar{Z} = \left(b_{2i}\, b_{2i-1} + \overline{b_{2i}}\,\overline{b_{2i-1}}\right).\left(b_{2i}\, b_{2i+1} + \overline{b_{2i}}\,\overline{b_{2i+1}}\right) \quad (6)$$

Boolean logic simplification of (6), results in:

$$\bar{Z} = b_{2i}\, b_{2i-1} b_{2i+1} + \overline{b_{2i}}\,\overline{b_{2i-1}}\,\overline{b_{2i+1}} \quad (7)$$

which demonstrates that when all three inputs have the same state, $\bar{Z}$ will have high logic value. With the help of (7) the circuit level implementation of encoder section has been illustrated in Fig. 1. In order to explain the design concept behind this structure, one can say that if $b_{2i+1}=0$, $\bar{Z}$ will be equal to $\overline{b_{2i}}\,\overline{b_{2i-1}}$ and this situation has been realized with the help of three transistors in series. Following the same procedure, if $b_{2i+1}=1$, then another branch consisting of three transistors in series can produce $b_{2i}\, b_{2i-1}$ output. Moreover, when the logic state of scaling factor X_i becomes zero, we have $\bar{Z}=0$ and a single NMOS transistor will be enough to produce the corresponding output.

To reduce total transistor count, the XOR gates which are generating X_1 and X_2 output can be

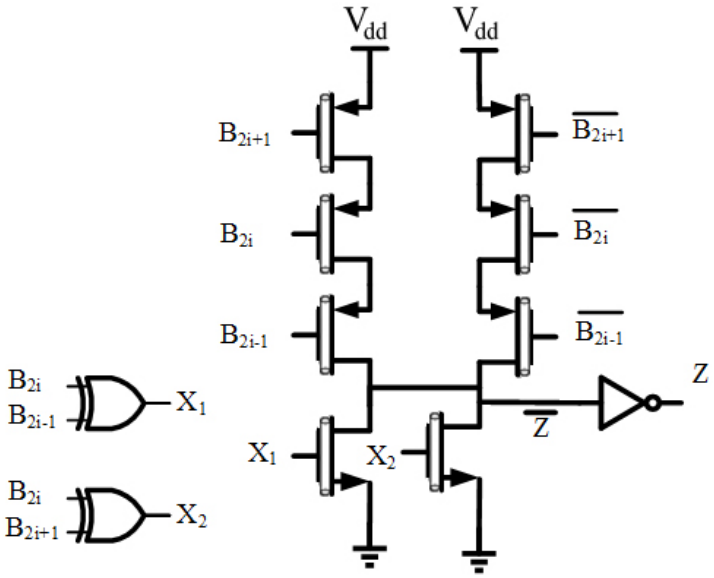


Fig. 1. Proposed scheme for Booth encoder.

implemented with non-full swing four transistor gates proposed in [25] since they are driving the gates having only NMOS transistor. Compared to design reported in [14] which has employed 10 transistor XOR/XNOR gates originally reported in [26], all of the full swing XOR and XNOR gates in this work have been implemented by means of 6 transistor gates described in [25]. Fig. 2 shows the redesigned XOR gates in CNTFET technology which are utilized in our scheme.

Moreover, the PMOS transistors that are fed by the inverted state of the inputs can be replaced by NMOS counterparts to save six transistors already used including those inside the inverters. By applying these techniques, the architecture of Fig. 3 will be obtained as the improved version of the proposed Booth encoder.

Compared with the circuitry of [14], two transistors have been reduced in the architecture of Booth encoder and the latency is reduced to less than two XOR gates which illustrates the advantages of proposed encoder section. For the decoder section, the circuit of Fig. 4 has been utilized which is derived from [14] employing the CNTFET technology in which the full swing XOR gates of Fig. 2 were employed.

To calculate gate-level delay from inputs to the outputs, it is clear that the critical path starts from encoder section where the parameter *Z* is being generated and ends in the PP where the gate of

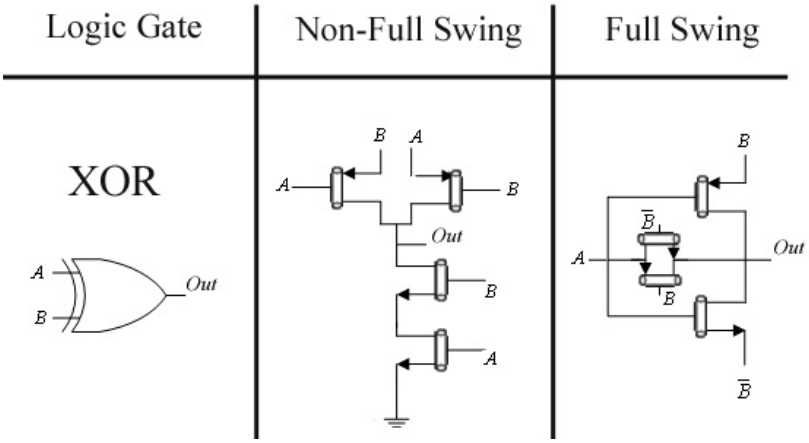


Fig. 2. Utilized XOR Gates in the design process (previously introduced in [25]).

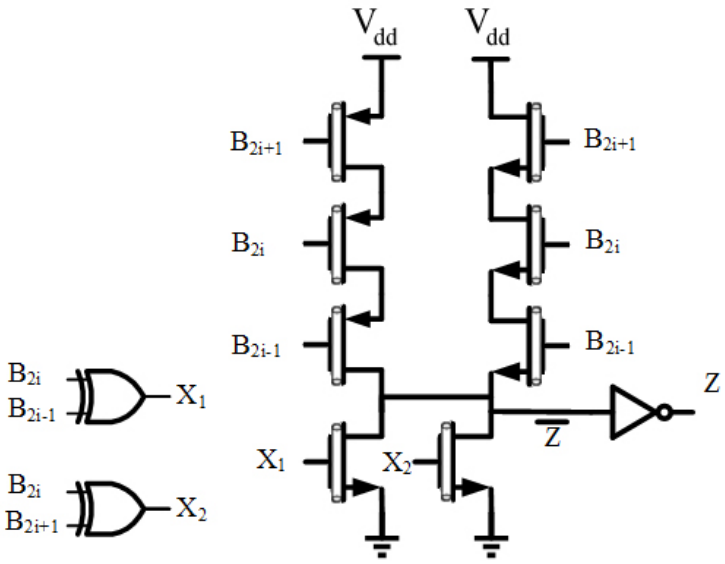


Fig. 3. Improved scheme of Booth encoder.

final Transmission Gate (TG) is fed by *Z* signal. Compared with [14], which has a gate level delay equal to two XOR logic gates plus one transistor, in the proposed scheme the delay has been reduced to less than two XOR gates considering the fact that the propagation delay for *Z* is equal to one XOR gate plus one inverter. In [15], although the gate level latency is claimed to be one XOR gate plus one transistor, the inverted state of the PP is obtained at the output node which needs an extra inverter to get the PP itself. Besides, in the design reported in [15], four parallel paths were used to produce the output while in the proposed architecture this problem is clearly improved by using two paths in parallel.

RESULTS AND DISCUSSIONS

A. Propagation Delay Evaluation

In order to have a better insight into the advantages of the proposed radix-4 scheme, the Elmore delay rule [27] has been employed to evaluate the propagation latency. By means of Elmore method, the time constants for different paths are examined and the largest value of the calculated time constant will determine the critical path delay. The corresponding propagation latency when the output signal reaches 50% of its final value will be 69% of the relevant time constant.

Considering the critical path for *Z*, the schematic of Fig. 5 can be used for calculation of delay in

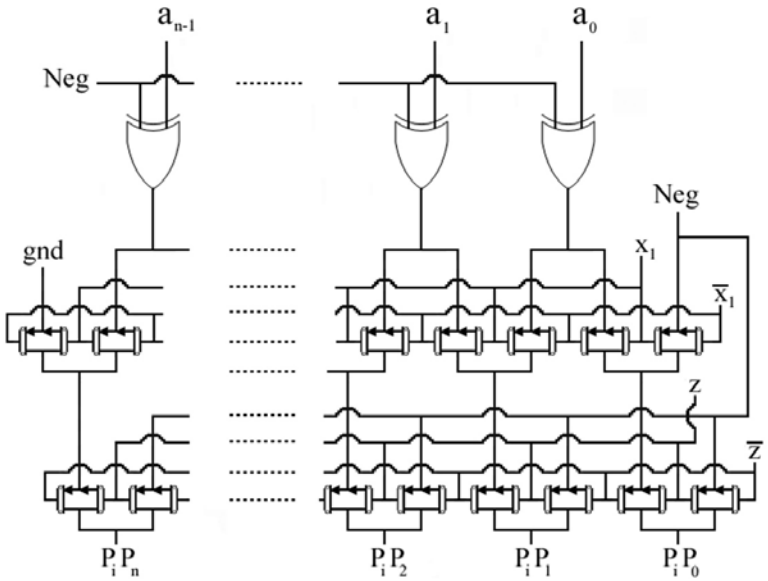


Fig. 5. Decomposition of proposed Booth scheme for delay calculation (a) path for (b) path for Z, and (c) decoder section.

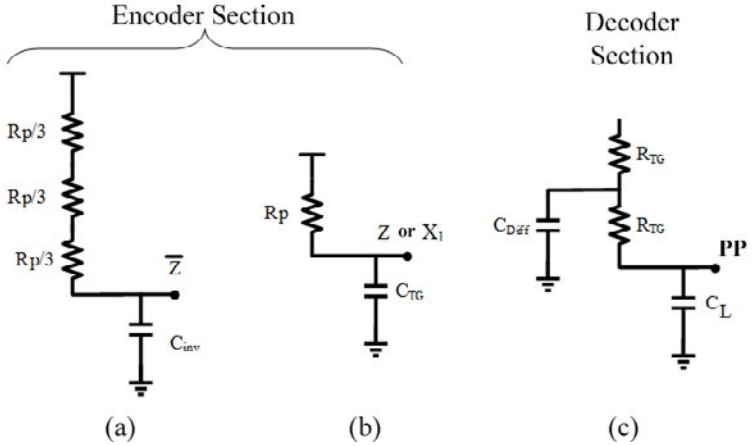


Fig. 4. Booth decoder derived from the work proposed in [14] using CNTFET.

which Fig. 5(a) demonstrates decomposition of the path for generation of $\bar{Z}$, while Fig. 5(b) shows the corresponding path for Z, X_1, and X_2 (because of having similar structure). Fig. 5(c) illustrates the decomposition of the decoder section in which C_{Diff} denotes the diffusion capacitance; since it has a minimal value, therefore, has been neglected in calculations.

By defining C_{inv} and C_{TG} as the corresponding capacitances for inverter and TG, respectively and by assuming that $C_{inv} = C_{TG}$, it is clear that there are two parallel paths for signal propagation. The first path starts from the inputs, produces $\bar{Z}$ and Z and faces one TG towards the output node. In the second path, the input signals propagate through one of the XOR gates (via X_1 or X_2) to the decoder circuit and reach the output node by passing through two TGs.

For the first path, the delay will be obtained by summing three individual time constants denoted by $\tau_{\bar{Z}}$, τ_Z and τ_{TG}. $\tau_{\bar{Z}}$ represents the time constant for the generation of $\bar{Z}$ and based on the architecture of Fig. 5(a) is equal to [28]:

$$\tau_{\bar{Z}} = \left(\frac{R_P}{3} + \frac{R_P}{3} + \frac{R_P}{3}\right) C_{inv} = R_P C_{inv} \quad (8)$$

where in this equation, R_P defines the equivalent resistance of PMOS transistor. For τ_Z which describes the time constant in which Z signal is being created, we have:

$$\tau_Z = R_P C_{TG} \quad (9)$$

Finally, τ_{TG} illustrates the time constant for signal propagation through a TG, which is equal to:

$$\tau_{TG} = R_{TG} C_L \quad (10)$$

which in this equation C_L characterizes the load capacitance. Summation of these latencies with the assumption of $C_{inv} = C_{TG}$ and $R_P = R_{TG}$, results in the propagation delay of the first path which is equal to:

$$\tau = \tau_{\bar{Z}} + \tau_Z + \tau_{TG} = 2R_P C_{TG} + R_P C_L \quad (11)$$

By applying the same procedure to the second path, the delay will be the summation of two time constants τ_X and $\tau_{decoder}$, where τ_X represents the time constant for either X_1 and X_2 outputs and $\tau_{decoder}$ illustrates the time constant for decoder section [28]. With the help of Fig. 5(b) τ_X can be written as:

$$\tau_X = R_P C_{TG} \quad (12)$$

By using Fig. 5(c) for the decoder section, the $\tau_{decoder}$ parameter is calculated as [28]:

$$\tau_{decoder} = R_{TG} C_{Diff} + (R_{TG} + R_{TG}) C_L \quad (13)$$

and because $C_{Diff} << C_L$ and $R_P = R_{TG}$, then (13) will be simplified as:

$$\tau_{decoder} \cong 2R_P C_L \quad (14)$$

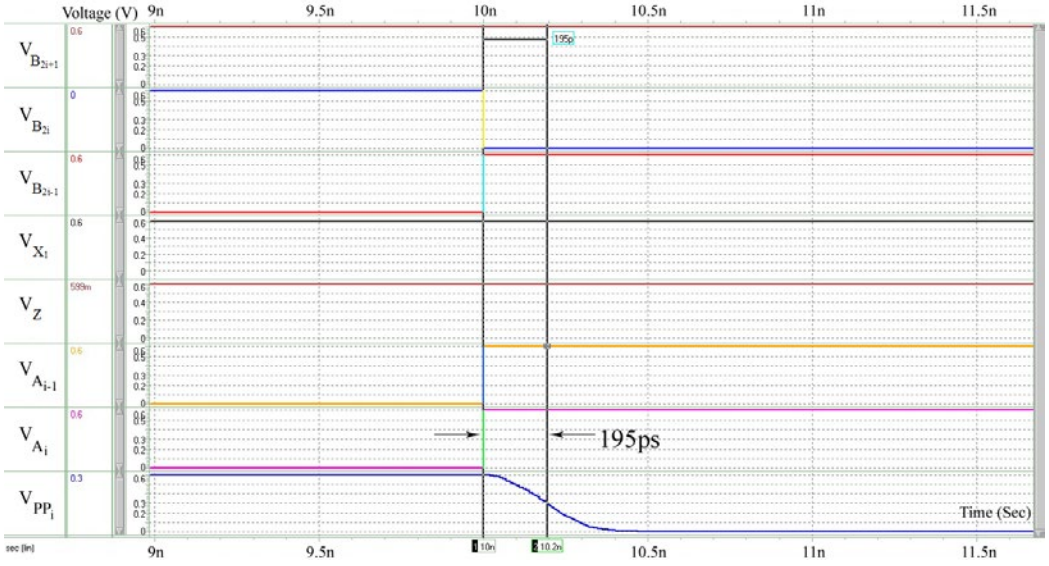


Fig. 6. Simulation results for the measurement of the delay of the proposed Booth scheme in CNTFET technology.

By adding these latencies, the propagation delay for the second path can be obtained which is equal to:

$$\tau' = \tau_X + \tau_{decoder} = R_P C_{TG} + 2R_P C_L \quad (15)$$

Considering the fact that the load capacitance will be the input capacitance of the PPRT in a parallel multiplier, C_L will has a value much greater than C_{TG}. As a result, $\tau' > \tau$, and the critical path will be determined by the second path.

B. Simulation Results

In order to measure the delay of the proposed radix-4 Booth scheme, the simulations have been carried out in HSPICE using the CNTFET32nm standard process having 0.6V power supply. Fig. 6 demonstrates the results, which indicate the correct functionality of the proposed architecture and shows a delay of about 195ps.

For a fair comparison between the proposed Booth scheme and the recently reported distinguished works in this field, the circuits reported in [12], [13], [14] and [15] are simulated in similar conditions along with the proposed design in this work to obtain the delay and power consumption of these designs. To achieve this, the same gates including the XOR gates of Fig. 2 were used in the architectures of simulated works while a capacitive load consisting of the 4-2 compressors from [26] was employed to provide a more realistic environment. The results, which are shown in Fig. 7 and Fig. 8 for the delay and power comparison, respectively, illustrate that the proposed Booth structure has less delay than the previous works; however, the design reported in [15] has the smallest power consumption.

Table 3 summarizes the comparison results based on simulations in CNTFET 32nm process. To interpret the results realistically, the Power Delay Product (PDP) was calculated for all these designs and is also added to the table for a better comparison. The PDP specification illustrates that our work has better performance than previous designs. It must be mentioned that all simulations are performed at the operating frequency of 100MHz.

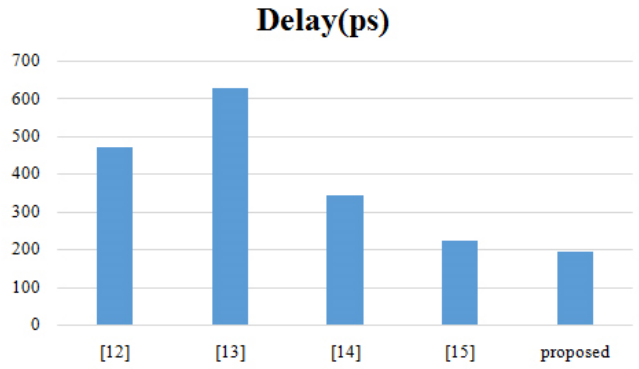


Fig. 7. Delay comparison of the proposed work and some recently reported designs on Booth scheme.

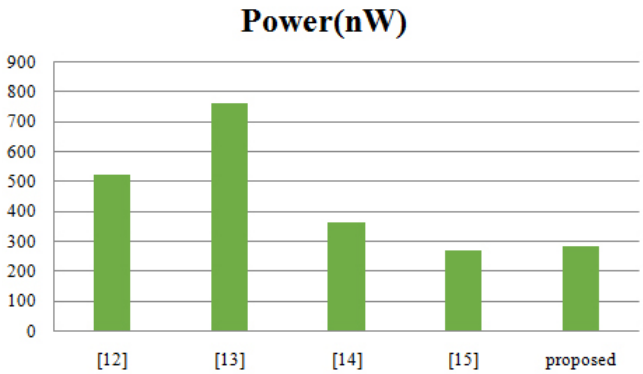
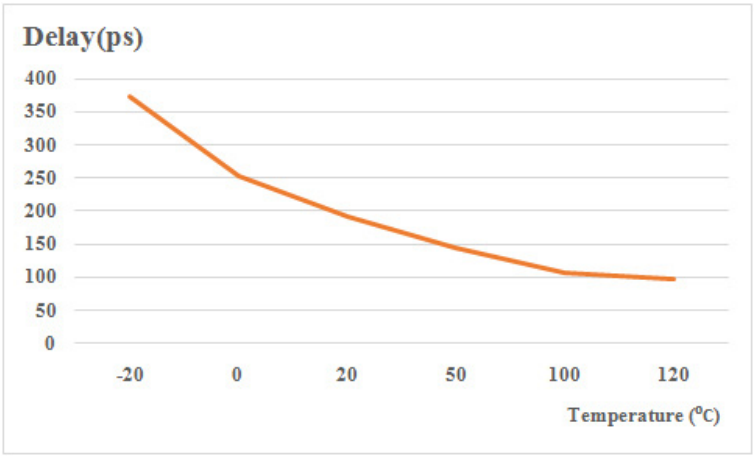


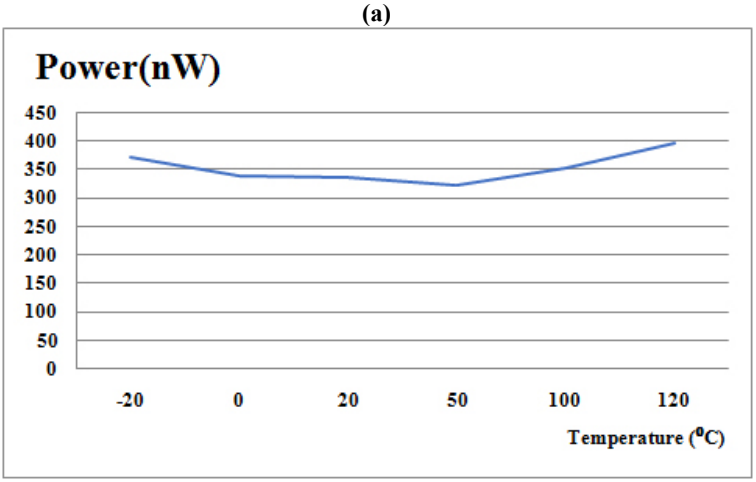
Fig. 8. Comparison of the power consumption for the proposed work and some recently reported designs on Booth scheme.

Table 3. Comparison of Proposed Scheme and Previous Works.

Work	This Work	[12]	[13]	[14]	[15]
Technology(nm)	32	32	32	32	32
Gate Level Delay	1.75	4	4	2.25	1.75
Delay(ps)	195	472	627	343	224
Transistor Count	44	54	54	46	43
Power Consumption(nW)	288	527	764	365	272
PDP(10^{-18})	56.16	248.744	479.028	125.195	60.928



(a)



(b)

Fig. 9. The effect of temperature changes on (a) delay of critical path (b) power consumption.

To investigate the correct behavior of the proposed circuit under different operating conditions, the temperature has been swept from -20°C to 120°C in CNTFET technology and the results have been shown in Fig. 9. Fig. 9(a) illustrates variations of the latency of critical path while the curvature of power dissipation versus temperature changes is presented in Fig. 9(b).

Finally, the supply voltage has been swept from 0.5V to 1.0V to demonstrate the changes in delay along with the variations of power supply. The result which is shown in Fig. 10 illustrates that the supply increment reduces the critical path delay.

CONCLUSIONS

In this manuscript, a novel and robust scheme for radix-4 Booth scheme has been presented which outperforms the previous works from the viewpoint of speed performance. Proposed in CNTFET technology, the main advantages of

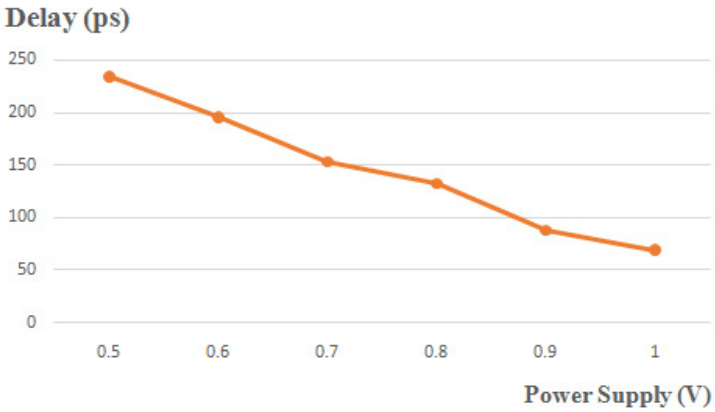


Fig. 10. Variations of critical path delay versus power supply changes.

the proposed scheme are its improved speed performance and power-delay efficient feature which makes it a very potential candidate to be used inside the high performance parallel multipliers. These improvements have been achieved by modifications applied to the encoder section using PTL which led to the decrement of middle stage capacitances while the analytic calculations show conformity with design considerations.

For evaluation of correct functionality, simulations using CNTFET 32nm standard process have been performed for the designed scheme, which depicts the latency of 195ps for the critical path. In addition, the comparison with previous works using PDP specification demonstrates the superiority of proposed structure over previous designs.

CONFLICT OF INTEREST

The authors declare that there are no conflicts of interest regarding the publication of this manuscript.

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