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ORIGINAL ARTICLE

Channel thickness dependency of high-k gate dielectric based double-gate CMOS inverter

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Abstract

This work investigates the channel thickness dependency of high-*k* gate dielectric-based complementary metal-oxide-semiconductor (CMOS) inverter circuit built using a conventional double-gate metal gate oxide semiconductor field-effect transistor (DG-MOSFET). It is espied that the use of high-*k* dielectric as a gate oxide in n/p DG-MOSFET based CMOS inverter results in a high noise margin as well as gain. It is also found that delay performance of the inverter circuit also gets upgraded slightly by using high-*k* gate dielectric materials. Further, it is observed that the scaling down of channel thickness (T_{Si}) improves the noise margin (NM), and gain (A) at the cost of propagation delay (P_d). Moreover, it is also observed that the changes in noise margin ($\Delta NM = NM_{(K=40)} - NM_{(K=3.9)}$), propagation delay ($\mathbf{\Delta P}_d = P_{d\,(K=40)} - P_{d\,(K=3.9)}$), and gain ($\mathbf{\Delta A} = \mathbf{A}_{(K=40)} - A_{(K=3.9)}$) gets hinder at lower T_{Si}. Therefore, it is apposite to look at lower channel thickness (~6 nm) while designing high-*k* gate dielectric-based DG-MOSFET for CMOS inverter cell.

Keywords: *Channel Thickness; CMOS; Double-Gate; High-k Dielectric; Inverter Cell.*

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INTRODUCTION

The performance improvement of Integrated circuits made a successful demand in semiconductor industries. This is achieved due to the continuous scaling of the semiconductor device which has been reached into the nanometer regime. Due to aggressive scaling of the device dimensions various short channel effects (SCEs) are in the limelight. In contrast to this, the multi-gate architecture is an effective approach owing more channels controllability which condenses SCEs as per reported literature [1-4]. In accordance with the device performance various hybrid topologies like a double gate (DG), triple gate, gate all around (multi-gate) MOSFETs were invented to reduce the SCEs.

Further, to follow the prediction of the international technology roadmap for semiconductor (ITRS), [5] recent research elaborates several device engineering schemes to enhance the performance of scaled devices with minimizing SCEs & maintaining the electrical characteristics constant. By this, the integration level of nano-electronic devices is enhancing linearly. However, the gate oxide layer silicon dioxide (SiO_2) is decreased to a few nanometer thicknesses thereby maintaining the device performance constant. If the thickness is scaled below 1 nm, quantum tunneling effects are the serious issues that dominate and arise problems in power consumption [6-8]. Technically these issues are overcome by owning high dielectric materials (high-*k*). The key merit preferring high-*k* materials for Nano-devices is that the thickness of the high-*k* dielectric materials increases with the same

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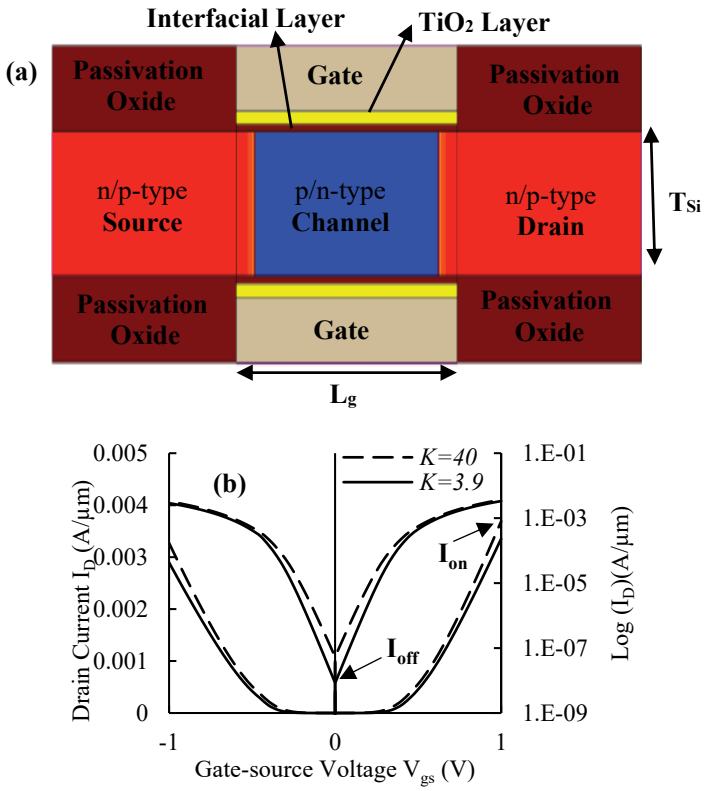

Fig. 1 (a) schematic view of n/p – type DG-MOSFET (b) I_D-V_{gs} curve of n/p – type DG-MOSFETs for SiO_2 (K = 3.9) and TiO_2 (K = 40).

capacitance. High-*k* dielectric materials induce a larger bandgap and larger dielectric constant. With this prominence, high-*k* materials are well suitable to improvise the device characteristics [9-11].

In this paper, the design of the double gate (DG) MOSFET has been used to investigate the effect of high-*k* gate dielectric on the digital performance of the complementary metal-oxide-semiconductor (CMOS) inverter circuit. The performance is analyzed in terms of propagation delay (P_d), inverter gain (A), low noise margin (NM_L), and high noise margin (NM_H) of a single-stage CMOS inverter circuit. Furthermore, the dependency of digital performance of high-*k* gate dielectric-based CMOS inverter cell built using DG-MOSFET on channel thickness (T_{Si}) is also investigated in this work. The organization of this paper is as: The paper starts with an introduction as section 1 and the device description with the simulation setup is elaborated in section 2. Section 3 presents the design and analysis of the DG-MOSFET based CMOS inverter circuit. Finally, the conclusion is drawn in section 4.

MATERIALS AND METHODS

The n/p-type double-gate (DG)-MOSFET structure is depicted in Fig. 1(a). 2D Sentaurus TCAD mixed-mode simulator [12] is used for simulating the DG-MOSFET. The channel thickness (T_{Si}) is speckled in the range of 6-14 nm for a fixed channel length (L_g) and interfacial layer thickness (T_I) of 30 nm and 0.2 nm respectively [13]. The Source/Drain doping concentration is set at 10^{20} cm^{-3} with arsenic (boron) for n-type (p-type). The channel region is uniformly doped with boron (arsenic) for n-type (p-type) at 10^{16} cm^{-3}. The titanium oxide (TiO_2) is used as high-*K* dielectric material (K = 40) for gate oxide to investigate the effect of the same on the performance of CMOS inverter [14]. The effective oxide thickness (EOT) is fixed at 1 nm throughout the study [15]. The physical thickness (T_{Phy}) for the TiO_2 is calculated as per $T_{Phy} = \{(EOT - T_I) \times K/3.9\}$. Table 1 tabulates the parameters used for the simulation of DG-MOSFET devices. Further, the Metal gate having a work function of 4.6 eV is utilized to dodge the poly-depletion effects [16].

Table 1. DG-MOSFET Parameter details.

Parameters	Value
Channel Length	30 nm
Interfacial Layer Thickness	0.2 nm
EOT	1 nm
Gate Dielectric Constant (*K*)	40
Source/Drain Doping	1×10^{20} atoms/cm^{-3}
Channel Thickness (T_{Si})	6-14 nm
Lateral Straggle (σ_L)	1 nm
Channel Doping	1×10^{16} atoms/cm^{-3}

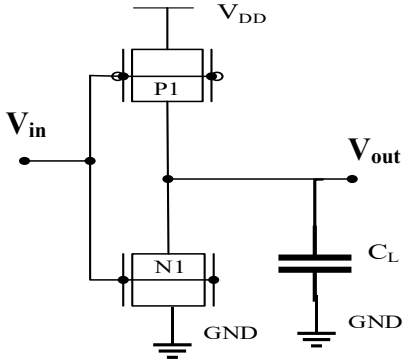

Fig. 2. DGMOSFET-based CMOS inverter circuit.

The saturation velocity (V_{Sat}) is set at 2.036 × 10^7 cm/s for the correct coupling of the carrier's transport phenomena [17-18]. A simulation study is executed using the following models: Philip unified mobility model, Lombardi mobility model, and band to band auger recombination, modified local density approximation (MLDA) quantization model to consider the quantum-mechanical effects in the device, old slotboom bandgap narrowing phenomenon, and SRH recombination/ generation model [19]. I_D–V_{gs} characteristics of n/p – type DG-MOSFET are in good calibration with the experimental data presented in our earlier work [20] and are reproduced as shown in Fig. 1 (b). Further, it can be observed from Fig. 1(b) that high-k gate dielectric results in improved on-current (I_{on}) but degrades the off-current (I_{off}).

RESULTS AND DISCUSSIONS

Fig. 2 displays the schematic view of a complementary metal-oxide-semiconductor (CMOS) inverter cell. The CMOS inverter circuit is executed with SiO_2 (k = 3.9) and TiO_2 (k = 40) based gate-stacked double-gate (DG)-MOSFET. The aspect ratio of p-type DG-MOSFET is made twice of n-type DG-MOSFET to match the current through both the transistors as can be verified from Fig. 1(b) [21].

It is a renowned fact that the device performance for digital applications leans on the on-current (I_{on}). Higher I_{on} will result in better delay performance [22]. Fig. 3 elucidates that the use of high-*k* dielectric as an alternative to SiO_2 for gate oxide increases the on-current (I_{on}), which can be attributed to improved delay performance of the CMOS inverter circuit. Furthermore, as observed in Fig 1(b), the high-*k* dielectric as gate oxide results in increased off current (I_{off}). This is attributed to an increase in power dissipation for TiO_2 based DG-MOSFET as compare to SiO_2 based DG-MOSFET as shown in Fig. 3.

The transfer, gain, and transient characteristics of high-*k* gate dielectric DG-MOSFET based CMOS inverter for SiO_2 and TiO_2 as gate oxide is compared

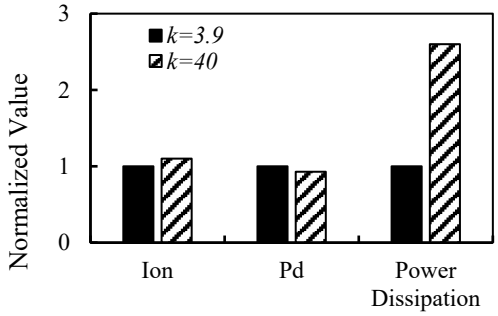

Fig. 3. Comparison of I_{on}, $P_{d,}$ and Power dissipation of DG-MOSFET built with SiO_2 & TiO_2 as a gate oxide.

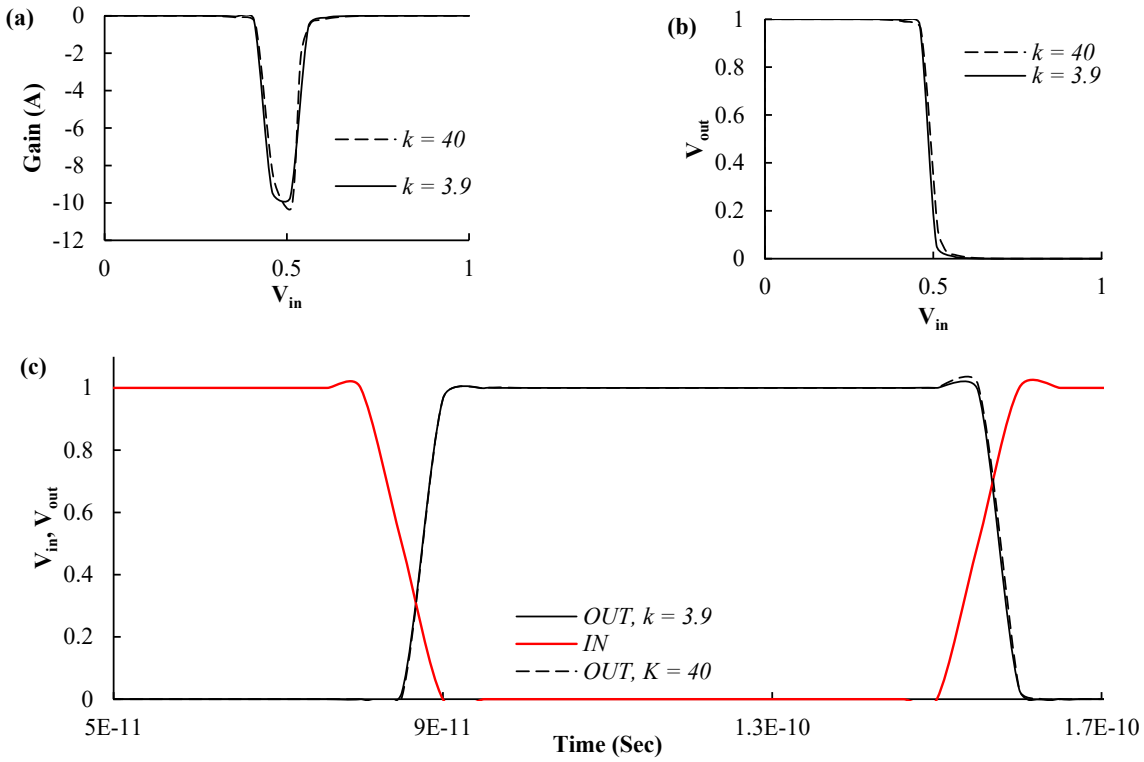

Fig. 4. (a) Transfer characteristic (b) Gain Characteristic (c) Transient Characteristic of DGMOSFET-based CMOS Inverter Circuit.

in Fig. 4(a), Fig. 4(b) and Fig. 4(c) respectively. It is found that the low noise margin NM_L and high noise margin NM_H of the inverter circuit can be increased by using TiO_2 material as gate oxide which may be attributed to improved DIBL of pull-up and pull-down transistor [23].

Further, large noise margins are not the only requirement. The regenerative property is another property that must be possessed by the inverter circuit to ensure that a distributed signal converges back to within the noise margins range after passing through several logical stages. Inverter Gain (A) is the parameter that can be used to quantify the regenerative property and can be given by differentiating the output voltage (Vout) with respect to input voltage (Vin) i.e.

$$A = \frac{dV_{out}}{dV_{in}}$$

Higher the gain (A), the better will be the regenerative property [21]. Improvement is observed in the gain (A) of the DG-MOSFET based CMOS inverter circuit by using high-*k* gate dielectric as shown in Fig. 4(b). Thus, for DG-

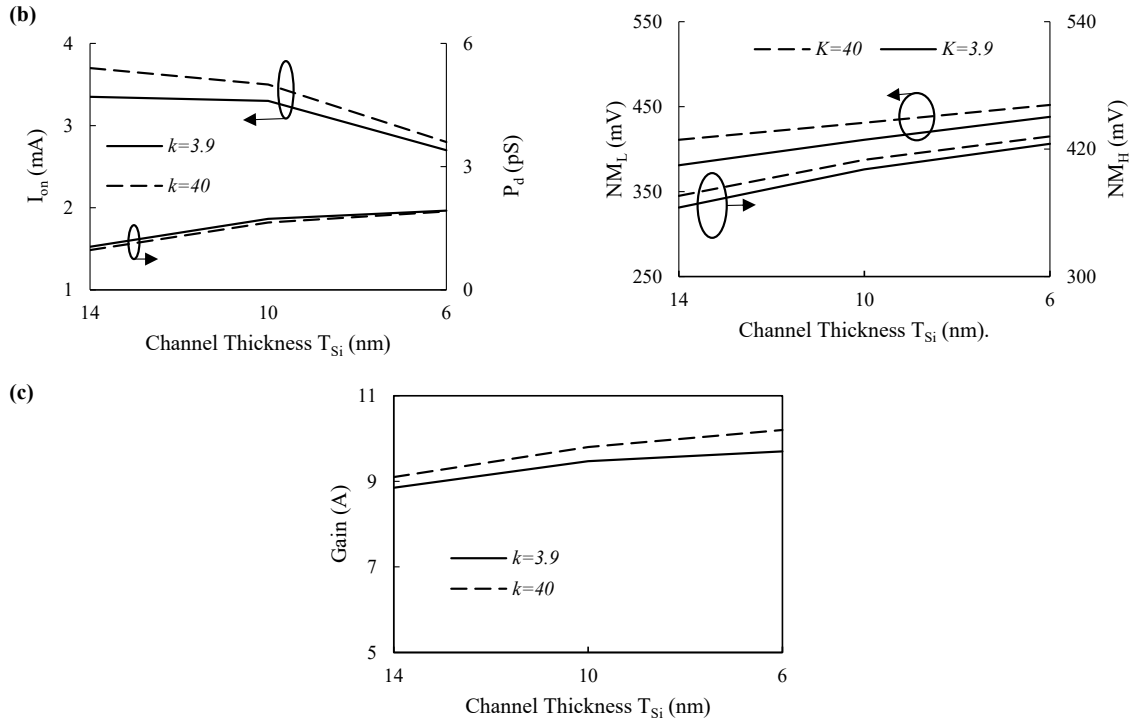

Fig. 5. (a) I_{on} & P_d v/s T_{Si} (b) NM_L & NM_H v/s T_{Si} (c) Gain (A) v/s T_{Si} for SiO_2 (k=3.9) & TiO_2 (k=40) as gate oxide.

MOSFET based CMOS inverter circuit, high-k gate dielectric-based devices are an attractive option. Furthermore, channel thickness (T_{Si}) is among the vital parameters for MOS designing, which impacts the performance behavior of high-k gate dielectrics [16]. The comparative enhancement in performance metrics of DG-MOSFET based CMOS inverter circuit realized with TiO_2 as compare to SiO_2 as gate oxide for various channel thicknesses is explained in the following subsection.

Channel Thickness (T_{Si})

The simulative analysis of DG-MOSFET based CMOS inverter circuit realized with SiO_2/TiO_2 as gate oxide collectively with channel thickness (T_{Si}) is been carried out and conferred in this subsection. The on-current (I_{on}) values of SiO_2 (k = 3.9) & TiO_2 (k = 40) gate oxide-based DG-MOSFET for various value of T_{Si} is plotted in Fig. 5(a). It is espied that, with downscaling of the T_{Si}, the I_{on} value decreases resulting in deprivation in delay performance (P_d) (Fig. 5(a)). Further, an improvement in low noise margin (NM_L) and high noise margin (NM_H) of the DG-MOSFET based CMOS inverter circuit is been observed with the scaling down of T_{Si}. The NM_L & NM_H for various values of T_{Si} is outlined in Fig. 5 (b). It is noticed that inverter gain (A) also gets improved with downscaling of T_{Si} (Fig. 5 (c)) which indicates that the inverter will show a better regenerative property at lower T_{Si}.

In our earlier work, we testified that the variation in channel thickness (T_{Si}) affects the outcome of the high-k gate dielectric on the performance of FinFET based 6T-SRAM cells [13]. Fascinatingly, it is espied that the variation in channel thickness (T_{Si}) also affects the outcome of the high-k gate dielectric on the performance of DG-MOSFET based CMOS inverter. In other words, change in performance metrics ($\Delta F = F_{K=40} - F_{K=3.9}$, where F is either P_d, A, or NM_L/NM_H) of DG-MOSFET based CMOS inverter realized with TiO_2 as gate oxide as compared to CMOS inverter realized with SiO_2 as gate oxide is T_{Si} dependent. The improvement in propagation delay (P_d) increases from ~ 2 % at T_{Si} = 6 nm to ~ 7 % T_{Si} = 14 nm (Fig. 6). Furthermore, Fig. 6 elucidates that the change in Noise Margins i.e. ΔNM_L & ΔNM_H, increases with scaling up of T_{Si} (2% & 1% respectively at T_{Si} = 6 nm and 7% & 10% respectively at T_{Si} =14 nm). However, the change in Gain (ΔA) decreases from 5% at T_{Si} = 6 nm to 2% at T_{Si} =14 nm.

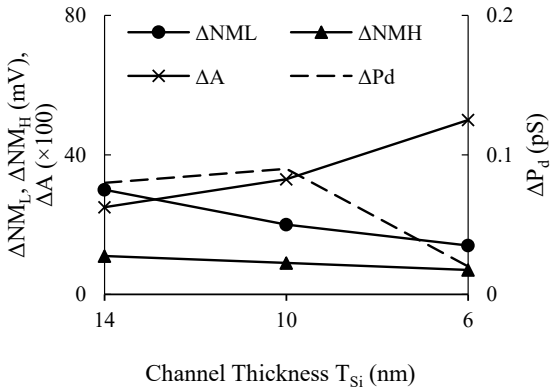

Fig. 6. ΔNM_L, ΔNM_H, ΔP_d & ΔA for the various value of T_{Si}.

CONCLUSION

The channel thickness dependency of DG-MOSFET based CMOS inverter circuit built using High-*k* gate dielectric material i.e. TiO_2 (*k* = 40) has been explored through extensive device simulations. It is espied that the performance matrices i.e. noise margin, delay, and gain of the DG-MOSFET based CMOS inverter circuit show improvement when SiO_2 is replaced by a high-*k* dielectric material (TiO_2) in the gate-stack configuration. It is also noticed that scaling down of channel thickness (T_{Si}) further improves the low & high noise margins (NM_L & NM_H), and gain (A) of the inverter circuit for both SiO_2 and TiO_2 gate dielectrics with negligible degradation in delay performance. However, the comparative improvement (ΔF) observed in performance matrices caused by high-*k* gate dielectric degrades with downscaling of channel thickness (T_{Si}) from 14 nm to 6 nm. It is also observed that ΔNM_L, ΔNM_H, & ΔP_d are aggravated from 7 %, 10 %, and 7 % respectively at T_{Si} =14 nm to 2 %, 1 %, and 2 % respectively at T_{Si} = 6. Accordingly, it is relevant to consider lower channel thickness (T_{Si} ~ 6 nm) when high-*k* gate dielectric-based DG-MOSFET is used for the designing of CMOS inverter circuit.

CONFLICT OF INTEREST

The authors declare that they have no competing interests.

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