Journal of Advances in Computer Research
Quarterly ISSN: 2008-6148
Sari Branch, Islamic Azad University, Sari, I.R.Iran
(Vol. 10, No. 4, November 2019), Pages: 27-36
www.jacr.iausari.ac.ir

Design and Analysis of a Fault Tolerant 3-Input Majority Gate in Quantum-dot Cellular Automata

Somayyeh Jafarali Jassbi[1], Farzaneh Jahanshahi Javaran[1], Hossein Khademolhosseini[✉2], Amir Sabbagh Molahosseini[3]

1) Department of Computer Engineering, Science and Research Branch, Islamic Azad University, Tehran, Iran
2) Department of Computer Engineering, Beyza Branch, Islamic Azad University, Beyza, Iran
3) Department of Computer Engineering, Kerman Branch, Islamic Azad University, Kerman, Iran
s.jassbi@srbiau.ac.ir; farzanejahanshahi@gmail.com; h.khademolhosseini@srbiau.ac.ir; amir@iauk.ac.ir

Received: 2020/01/08; Accepted: 2020/08/14

Abstract

QCA is a kind of computational technology used for developing circuits in Nano sizes. Decreasing the dimensions of pieces has led to the increase of circuit sensibility and quantum circuits are more vulnerable to defects and radiations of the environment. Majority gate and NOT gate (inverter) are the two basic gates in QCA technology based on which almost all circuits are made. So far, a limited number of fault-tolerant majority gates have been presented and research in this particular field seems appropriate. In this research we intend to provide a comprehensive design of 3-input majority gate in quantum cellular automata for all possible faults: misalignment, missing, dislocation, and redundancy so that low overhead is added to circuit. The gate is made up of both 90-degree and 45-degree cells. The results of this study indicate that our proposed 3-input majority gate is more fault-tolerant to the defects compared to the formerly presented one.

Keywords: *Nano-Electronics, Quantum-Dot Cellular Automata, Majority Gate, Fault Tolerance*

1. Introduction

Technology is improving every day and power usage of electronic devices is one of the most important things in this trend and the producers are always looking for the most possible performance with the least power usage and the smallest size.

Researchers believe when the size of transistors reduces to nano scale, undesirable effects like increased power consumption appear. So in near future, advancement of transistor-based electronic industries will be stopped and currently we are forced to seek for a deserving alternative to silicon technology. In comparison with the present technology, the candidates are expected to be of lower power consumption and higher speed and more important, they have to get rid of problems common in silicon transistors in nano dimensions. Among the solutions, Quantum-dot Cellular Automata (QCA) is one promising technology [1-4].

QCA is a kind of computational technology used for developing circuits in nano sizes. In this research we intend to design a 3-input majority gate in quantum cellular automata capable of functioning correctly in presence of defects leveraging low overhead. Up to now, most of the presented fault tolerant layouts are made by cellular overhead however

we are to find a defect tolerant design just with applying a specific arrangement of cells. There are little researches on this area and hence working on this field is attractive.

In order to test the tolerance of the proposed design, first we apply the four possible faults misalignment, missing, dislocation and redundancy to the gate and then we analyze acting of the gate using simulation cad tool QCADesigner.

Due to the importance of designing fault tolerant circuits in QCA and researching on fault tolerant majority gate, studies on this topic is expanding [5]. Since different defects may occur, different fault tolerant gates have been introduced each related to a particular group. Till now, a limited number of fault tolerant 3-input majority gates have been introduced and researching on this topic seems appropriate. Two fault tolerant 3-input majority gates have been proposed in [6] and [7] and the corresponding tolerance of the gates against different types of single faults are investigated in these researches. Investigations show that these gates work better in cell missing fault in comparison with other faults.

2. Materials and methods

2.1. Primary Concepts of QCA

A QCA cell consists of four cavities (dots) which are set as a square near each other and two additional electrons which can move freely between the cavities. Based on Coulomb's law of repulsion, the location of these two electrons in cavities is diagonal in opposite corners and hence, two structures might occur. These two structures show two polarizations +1 and -1 which are assigned to logics 1 and 0, respectively (Figure 1) [8-11].

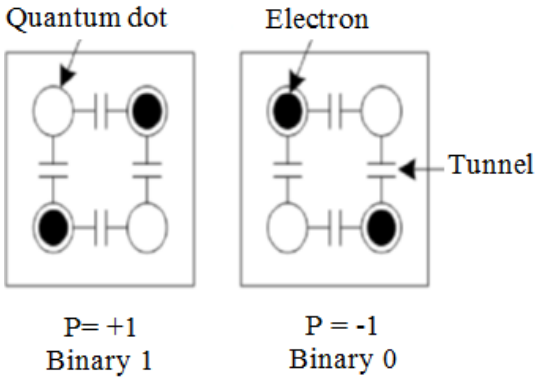

Figure 1. QCA Cell

QCA has a clock mechanism. Clock is an electronic factor which controls electrons movements in cells. Actually, clock makes different parts work simultaneously. As illustrated in Figure 2, in order to correctly propagate data and control switches between quantum cells, four clocking areas are used: Switch, Hold, Release and Relax [5].

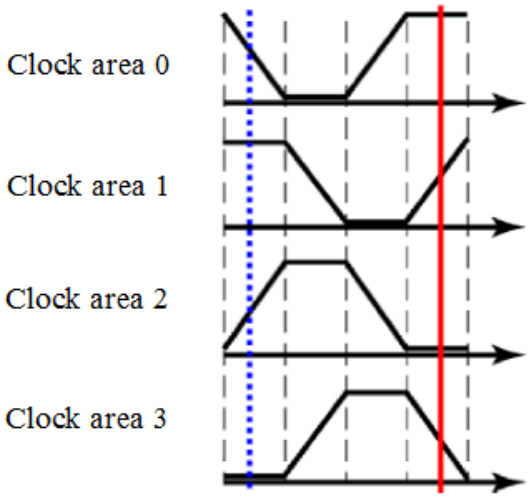

Figure 2. Four clock signals necessary for controlling QCA circuits

Majority gate and NOT gate (inverter) are the two basic gates in QCA technology based on which almost all circuits are made. Figure 3 shows a QCA inverter [12].

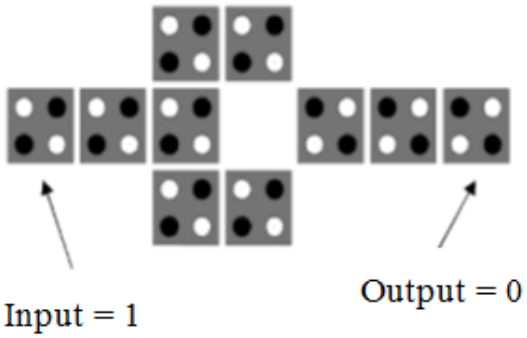

Figure 3. QCA inverter

In majority gate, the output always shows the majority among the input signals [13-17]. The structures and the schematics of basic 3 and 5 input majority gates are shown in figures 4 and 5, respectively.

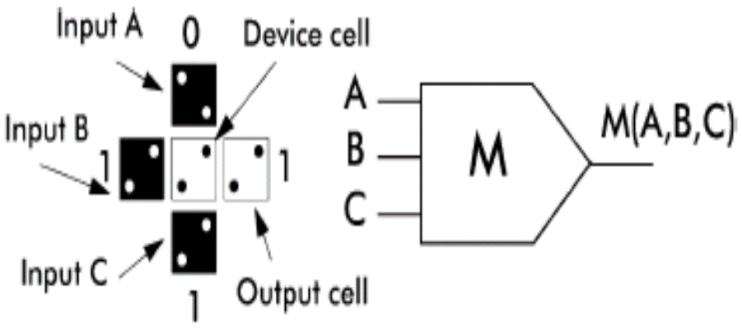

Figure 4. 3-input majority gate and its schematic

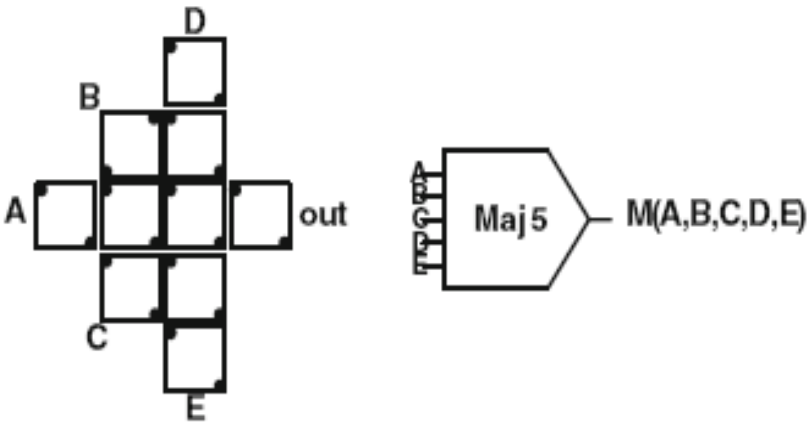

Figure 5. 5-input majority gate and its schematic

2.2 Fault types in QCA

The possible defects in a QCA circuit are as follows [5], [18-22]:

- Misalignment: a quantum cell is moved in its original direction.
- Missing cell: a cell is removed from the circuit.
- Dislocation: a cell is rotated proportionate to its adjacent cells.
- Redundant cell: when locating cells, one or more additional cells may be added to the circuit.

3. The proposed fault tolerant 3-input majority gate

The proposed layout for 3-input majority gate is shown in Figure 6. The design contains 16 cells in an area of 13524 square nanometers. From structural point of view, the simultaneous existence of rotated and standard cells leads to significant tolerance in this gate. Input cells A, B and C are joined to the 45 degree cells and the circuit output is produced through cell O.

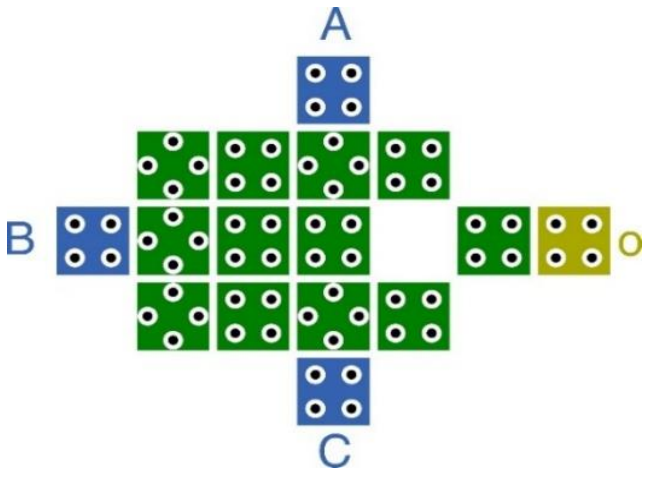

Figure 6. The proposed fault tolerant 3-input majority gate

To check the accuracy of the circuit, Coherence Vector simulator engine of QCADesigner software version 2.0.3 is utilized. The parameters listed in table 1 are applied in the simulation. As shown in figure 7, the output functions correctly in all the input patterns from 000 to 111 after 0.25 clock cycles.

Table 1. Parameters applied to Coherence Vector simulation engine

Parameter	Quantity
Cell size	18*18 nm^2
Dot diameter	5 nm
Centre-to-centre distance	20 nm
Temperature	2.000000 K
Relaxation time	4.1356675e-14 s
Time Step	1.000000e-016 s
Total Simulation Time	7.000000e-011 s
Clock High	9.800000e-022 J
Clock Low	3.800000e-023J
Clock shift	0.000000e+000
Clock Amplitude Factor	2.000000
Radius of Effect	80.000000 nm
Relative Permittivity	12.900000
Layer Separation	11.500000 nm

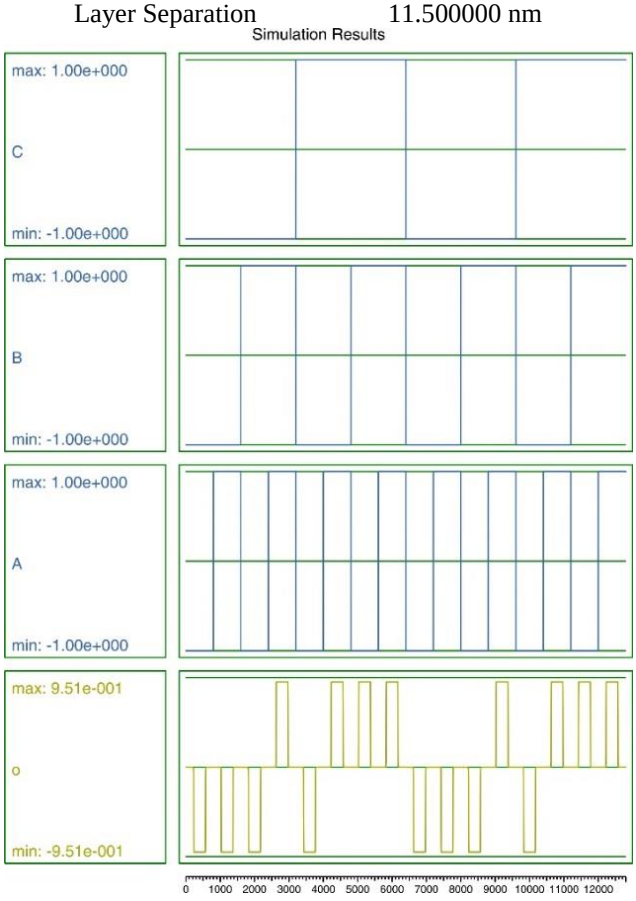

Figure 7. The simulation result of the proposed fault tolerant 3-input majority gate

As shown earlier in Figure 6, our proposed design for 3-input majority gate is made up of 16 QCA cells. It is worth noting that all the cells are arranged in a single layer.

3.1 Fault Tolerance Analysis of the proposed gate

As depicted in figure 8, in order to apply dislocation, missing and misalignment faults to the proposed circuit, all the body cells are considered as cells under test and are numbered.

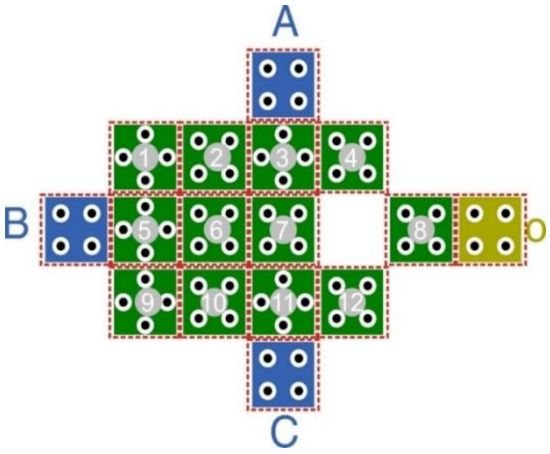

Figure 8. The proposed fault tolerant 3-input majority gate (numbered cells)

3.1.1 Misalignment Analysis

The results of misalignment fault analysis are shown in Table 2. As listed, all the 16 cells of the proposed gate are investigated as test cells in the four directions of North, South, East and West. Maximum tolerated amount of misalignment in the arrangement is evaluated for each cell. Since input cells are of great importance, analysis of the two cells A and B are explained here. Cell A can move 2 nanometers to West and East (horizontal movement) and on the other hand 1 and 3 nanometers movement are tolerated in vertical direction. Also, cell B is allowed to move 18 nanometers to the two directions of North and South and 20 nanometers to West which raises tolerance of the gate against misalignment fault significantly.

It is worth noting that the 5-nanometer tolerance of the output cell in directions of North and South and 6-nanometer tolerance of East have raised the drive capability of the gate to a great extent and therefore the overall tolerance of the circuit has been increased.

Table 2. Maximum tolerated misalignment of the cells

Cell	Vertical Movement (North)	Vertical Movement (South)	Horizontal Movement (East)	Horizontal movement (West)
A	3	1	2	2
B	18	18	1	20
C	3	1	2	2
O	5	5	6	1
1	2	1	1	2
2	2	1	1	1
3	1	1	1	1
4	10	5	11	1
5	1	1	1	1
6	1	1	1	1
7	1	1	15	1

8	6	6	1	6
9	1	2	1	2
10	1	2	1	1
11	1	1	1	1
12	5	10	11	1

3.1.2 Missing Cell Analysis

As shown in Table 3, tolerance of the proposed gate against missing fault is investigated via evaluating the output. The output wave resulted from simulation after removing each cell is compared with the form of the wave resulted from a fault-free gate. Investigating the 12 inner cells, missing of 7 single cells does not affect the output. Therefore, the percentage of missing fault tolerance can be considered 58%.

Table 3. Analysis of missing tolerance

Cell	Output (O)
1	Not changed
2	Changed
3	Not changed
4	Changed
5	Not changed
6	Not changed
7	Not changed
8	Changed
9	Not changed
10	Changed
11	Not changed
12	Changed

3.1.3 Dislocation Analysis

Dislocation fault evaluation is also done in QCADesigner through changing the type of cell from 90 degree to 45 degree or vice versa. As listed in Table 4, again 12 cells are investigated however only 2 cells show suitable tolerance against this fault. So it can be concluded that the proposed gate is not properly tolerant to dislocation fault and the tolerance percentage is 16.6%.

Table 4. Analysis of dislocation tolerance

Cell	Output (O)
1	Changed
2	Changed
3	Changed
4	Changed
5	Not changed
6	Not changed
7	Changed
8	Changed
9	Changed
10	Changed
11	Changed
12	Changed

3.1.4 Cell Redundancy Analysis

In order to analyze cell redundancy fault, figure 9 is drawn. The 5-by-7 rectangle shows all possible locations for cell redundancy. 10 locations are chosen and numbered. The other locations are similar to these 10 ones due to symmetry. Table 5 shows the tolerance analysis of the gate to cell redundancy fault. The process starts with adding a cell adjacent to the circuit and continues with simulating and comparing the result with the fault-free waveform. Adding cells to sensitive points 3, 4, 6 and 7 lead to change in the output. Hence, tolerance percentage of the proposed gate is 60%.

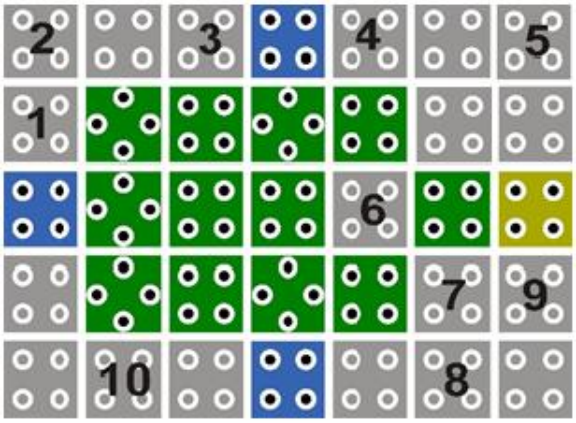

Figure 9. The possible locations for redundant cell and the selected ones

Table 5. Analysis of cell redundancy tolerance

Cell	Output (O)
1	Not changed
2	Not changed
3	Change
4	Change
5	Not changed
6	Change
7	Change
8	Not changed
9	Not changed
10	Not changed

3.2 Comparison

In [6] the authors have suggested a fault tolerant 3-input majority gate. The gate contains 13 quantum cells and in an area of 9604 square nanometers with 0.5 clock cycles delay and 63% of the faults are tolerated. The gate functions better in presence of additional cell than other faults.

The reference [7] has presented another fault tolerant design for 3-input majority gate. The gate is composed of 43 quantum cells and in an area of 38804 square nanometers with 0.25 clock cycles delay and 79% fault tolerance is obtained.

The fault tolerant design proposed in [14] for 3-input majority gate has 9 cells which occupy 9604 square nanometers. Its propagation delay and average fault tolerance are 0.5 cycles and 58%, respectively.

In Table 6, the proposed gate is compared with the designs presented in [6], [7] and [14]. As it is clear, our gate excels the others in terms of cost which is calculated using the following formula [15]:

$$Cost_{Area-Delay} = A \times T^n, \quad 0 \le n \le 2 \tag{1}$$

Our gate provides an acceptable fault tolerance by imposing low cost and hence it has balanced the tradeoff between fault tolerance and cost.

Table 6. Structural and fault tolerance comparison

Gate	Area (nm^2)	Cell Count	Clock Cycles	Cost	Average Fault Tolerance
Proposed gate	13524	16	0.25	3381	45%
The gate in [6]	9604	13	0.5	4802	63%
The gate in [7]	38804	43	0.25	9701	90%
The gate in [14]	9604	9	0.5	4802	58%

4. Conclusion

In this research a new fault tolerant 3-input majority gate has been designed using hardware redundancy method in QCA technology. In addition to structural analysis, the analysis of gate tolerance has been performed with applying the four fault types: misalignment, missing, dislocation and redundancy and the accuracy of gate operation has been tested using QCADesigner simulation tool. The proposed gate is composed of 16 cells which occupy 13524 nm^2 with 1 phase propagation delay and 45% average fault tolerance is provided. The cost of the 3-input majority gate is 3381 which is the lowest among the similar designs. Thus, the proposed majority gate maintains a balance between the tolerable fault and the imposed cost.

References

[1] International Technology Road map for Semiconductors, (2009), http://www.itrs.net/Links/2009ITRS/Home2009.htm.

[2] C.S.Lent, P.D.Tougaw, W.Porod, and G.H.Bernstein, "Quantum cellular automata," Nanotechnology, vol.4, no.1, pp.49–57, 1993.

[3] P. D. Tougaw and C. S. Lent, "Dynamic behavior of quantum cellular automata," Journal of Applied Physics, vol. 80, pp. 4722-4736, 1996.

[4] W. Porod, "Quantum-dot devices and quantum-dot cellular automata", Inter. J. Bifurcation and Chaos, vol. 7, no. 10 pp. 2199-2218, 1997.

[5] A. Roohi and H. Khademolhosseini, "Quantum-dot cellular automata: computing in nanoscale," Reviews in Theoretical Science, vol. 2, pp. 46-76, 2014.

[6] R. Farazkish, S. Sayedsalehi, and K. Navi, "Novel design for quantum dots cellular automata to obtain fault-tolerant majority gate," Journal of Nanotechnology, vol. 2012, 2012.

[7] B. Sen, M. Dutta, R. Mukherjee, R. K. Nath, A. P. Sinha, and B. K. Sikdar, "Towards the design of hybrid QCA tiles targeting high fault tolerance," Journal of Computational Electronics, vol. 15, pp. 429-445, 2016.

[8] C.S.Lent, P.D.Tougaw, "A device architecture for computing with quantum dots," Proceedings of the IEEE , vol.85, no.4, pp.541-557, Apr 1997.

[9] P. D. Tougaw and C. S. Lent, "Logical devices implemented using quantum cellular automata," Journal of Applied physics, vol. 75, pp. 1818-1825, 1994.

[10] W. Wang, K. Walus, and G. A. Jullien, "Quantum-dot cellular automata adders," in Nanotechnology, 2003. IEEE-NANO 2003. 2003 Third IEEE Conference on, 2003, pp. 461-464.

[11] R. K. Kummamuru, A. O. Orlov, R. Ramasubramaniam, C. S. Lent, G. H. Bernstein, and G. L. Snider, "Operation of a quantum-dot cellular automata (QCA) shift register and analysis of errors," Electron Devices, IEEE Transactions on, vol. 50, pp. 1906-1913, 2003.

[12] M. Kamrani, H. Khademolhosseini, A. Roohi, and P. Aloustanimirmahalleh, "A novel genetic algorithm based method for efficient QCA circuit design," in Advances in Computer Science, Engineering & Applications, ed: Springer, 2012, pp. 433-442.

[13] H. Khademolhosseini and Y. Nemati, "A New Design for Two-input XOR Gate in Quantum-dot Cellular Automata," Journal of Advances in Computer Research, vol. 10, pp. 1-8, 2019.

[14] H. Khademolhosseini, S. Angizi, and Y. Nemati, "A Fault-Tolerant Design for 3-Input Majority Gate in Quantum-Dot Cellular Automata," Journal of Nanoelectronics and Optoelectronics, vol. 13, pp. 93-103, 2018.

[15] W. Liu, L. Lu, M. O'Neill, and E. E. Swartzlander, "A first step toward cost functions for quantum-dot cellular automata designs," IEEE Transactions on Nanotechnology, vol. 13, no. 3, pp. 476-487, 2014.

[16] A. N. Bahar and K. A. Wahid, "Design of an Efficient N× N Butterfly Switching Network in Quantum-Dot Cellular Automata (QCA)," IEEE Transactions on Nanotechnology, vol. 19, pp. 147-155, 2020.

[17] J. Pal, S. Bhattacharjee, A. K. Saha, and P. Dutta, "Study on Temperature Stability and Fault Tolerance of Adder in Quantum-dot Cellular Automata," in 2019 5th International Conference on Signal Processing, Computing and Control (ISPCC), 2019: IEEE, pp. 69-74.

[18] M. R. Gadim and N. J. Navimipour, "A new three-level fault tolerance arithmetic and logic unit based on quantum dot cellular automata," Microsystem Technologies, vol. 24, pp. 1295-1305, 2018.

[19] R. Farazkish, "Novel efficient fault-tolerant full-adder for quantum-dot cellular automata," International Journal of Nano Dimension, vol. 9, pp. 58-67, 2018.

[20] S. S. Ahmadpour and M. Mosleh, "A novel fault-tolerant multiplexer in quantum-dot cellular automata technology," The Journal of Supercomputing, vol. 74, pp. 4696-4716, 2018.

[21] H. Bandani Sousan, M. Mosleh, and S. Setayeshi, "Designing and implementing a fast and robust full-adder in quantum-dot cellular automata (QCA) technology," Journal of Advances in Computer Research, vol. 6, no. 1, pp. 27-45, 2015.

[22] Z. Mohammadi and M. Mohammadi, "Fault Tolerant Reversible QCA Design using TMR and Fault Detecting by a Comparator Circuit," 2011.