Full Adder and Full Subtractor Design in Quantum Cellular Automata

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ABSTRACT:
Quantum Cellular Automata (QCA) is an alternative promising nanotechnology for semiconductor transistor based technology. QCA benefits from several features such as high speed, low power consumption and can be used for extremely dense structures. One of the important issues in arithmetic circuits is design of full adder/full subtractor (FA/FS respectively). Our main contribution in this paper is proposing a one-bit FA/FS which benefits from less cell counts compared to the state-of-the-art technologies. The proposed QCA FA/FS ameliorate the number of cells in comparison with the best FA/FS studied in the literature. As well as the mentioned feature, temperature analysis of suggested circuit shows that our design is more tough compared to the previous works.

Keyword: Quantum Cellular Automata (Qca), Low Power Consumption, Arithmetic Circuit, Full Adder/Full Subtractor.

1. INTRODUCTION

Nowadays, the nanometer scale CMOS technology is involved with problems such as short channel effect, high power consumption and high cost of lithography [1]. Therefore, several possible technologies such as Single Electron Transistor (SET), Carbon Nanotube Field Effect Transistor (CNFET) and Quantum Dot Cellular Automata (QCA) have been emerged. Quantum cellular automata has attracted a lot of attention due to its interesting features such as low power consumption, high speed switching and small dimension [2]. The basic QCA cell, that is able to represent binary data, consists of two electrons and four quantum dots.

Many efforts have been done about the sequential and combinational circuits gradually. The most efficient implementation of the basic circuit such as full adder is important. Different designs by the aim of reduction of area, power consumption and speed enhancement are discussed in [3][4][5][6]. In this paper, a new one bit FA/FS is introduced which operates in higher speed and lower area in comparison with its counterparts [7][8].

The rest of this paper is organised as follows. Section 2 reviews the basic concept of QCA. In Section 3 a new design for FA/ FS is proposed. Also the layout of the proposed circuit is declared. Simulation results and circuit evaluations is demonstrated in section 4 and the last section concludes the paper.

2. QCA BACKGROUND

QCA cells are the basic element of QCA circuits and contains four quantum-dots positioned at the corner of square structure. Each cell has two electrons which can move between the mentioned dots. Due to columbic repulsion, the electrons occupy two opposite corners of the cell. Consequently, each cell has two steady states so these states can represent binary encoding. In each location, the density of each particle is computed by the wave equation and polarization parameter.Two ground states of a QCA cell is shown in Fig. 1 [9].

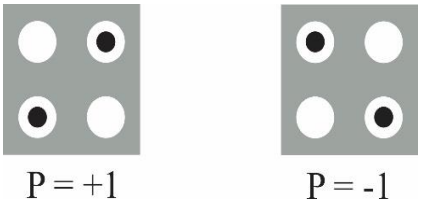

Fig. 1. Two basic QCA cell and pola rization of Cell.

In QCA technology, the information flow is

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controlled and synchronized by for clocking signal. In addition, energy signal is provided by power supply in each stage. Where each of them is shifted 90-degree compared to previous signal. Each clock signal has four phases that is shown in Fig. 2.

The barrier energy is demonstrated in four phases (switch, hold, release and relax). Different phases are increased pipelining attribute in the QCA circuit. Therefore, the pipelined circuit is proper option for QCA-based designs [10].

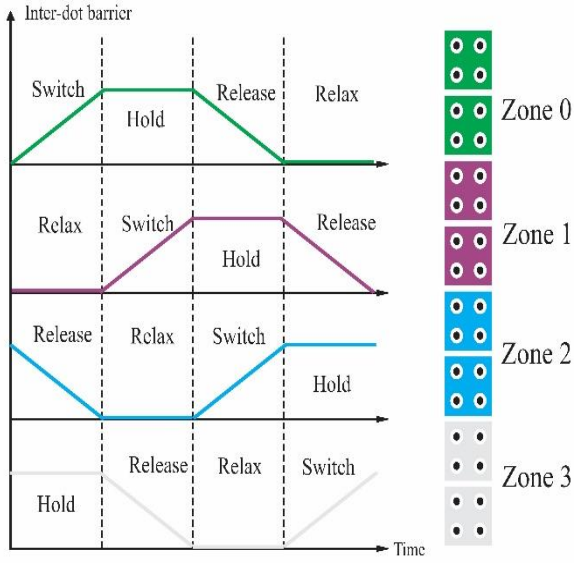

Fig. 2. Clock phases in QCA with clock zone.

In QCA architecture, logical gates and wire structure are constructed by the cells. If a cells are placed together, cells would impress their neighboring cells and consequently cell polarization is propagated until the last cell [11].

Inverter gate is the basic elements in QCA structure. As its name implies, inverter gate reverses logic input. In Fig. 3(a), inverter gate is depicted. Actually, since the input cell is placed diagonally toward output cell, output logic cell is opposed to the input logic.

Another gate which is used in QCA circuits is majority gate. In this gate, majority logic of inputs is transferred to the output. Today one design for three input majority is presented as shown in Fig. 3(b). A, B and C are the input cells which are the result of the votes carried to output cell through the device cell. Logical function of majority gate is illustrated in Eq. 1. Two-input AND gate and two-input OR gate are made by applying fixed polarization to one of the inputs. For example, if C is fixed to -1, majority gate behaves like two-input AND gate, and if C is fixed to 1, majority gate will be two-input OR gate [12].

$$\text{Majority3 (A, B, C)} = AB + AC + BC \quad (1)$$

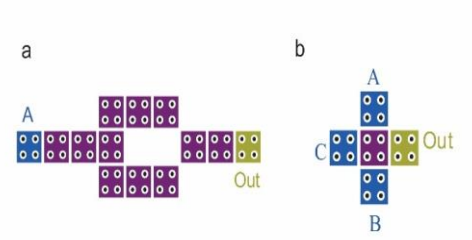

Fig. 3. Basic Gate (a) Inverter (b) Three input majority gate.

The FA cell and FS cells are the basic elements of arithmetic circuits such as multiplier, divider and more complex circuits. So far, many efforts have been made to design an efficient basic circuit [13][14][15][16].

3. DESIGN APPROACH

Several designs of FA and FS as arithmetic units are presented in the literature that each of them proposes plan exposed features. A FA cell has two outputs (carry-out and sum) and also a FS cell has two output (borrow-out and sub) which are realized by this circuit. The Eqs. 3, 4. indicate the formulas of these circuits.

For a FA we have:

$$Sum = A \oplus B \oplus C$$
$$Carry - Out = AB + AC + BC \quad (2)$$

Also for a FS we have:

$$Sub = A \oplus B \oplus C$$
$$Borrow - Out = A\overline{B} + AC + \overline{B}C \quad (3)$$

In arithmetic units, each circuit which provides combined outputs is favorable for designers. Table 1 demonstrates the truth table of a one-bit FA/FS. In this paper, a FA/FS design in small only one circuit is discussed. Three majority gates and two inverters are used for implementation that it reduces the number of majority gates compared to the previous works. Due to the fact that the number of majority gates has been diminished, the power consumption and cell counts are reduced. The mentioned reduction in the number of gates is due to using the borrow-out in gaining of the third output.

Table 1. Truth Table of a full adder and full subtractor.

A	B	C	Carry-out	Borrow-Out	Sum=Sub
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	1	0	0
1	1	1	1	1	1

Eq. 5 is used to compute carry-out, borrow-out, sum and sub bits in the proposed circuit. Also the schematic diagram of one-bit FA/FS is illustrated in Fig. 4.

$$Carry - Out = maj(A, B, C)$$
$$Borrow - Out = maj(\bar{A}, B, C)$$
$$Sum = Sub = Maj(\overline{Carry - Out}, Borrow - Out, A) \quad (4)$$

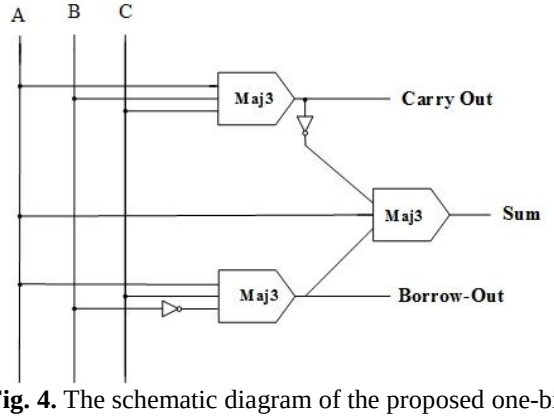

Fig. 4. The schematic diagram of the proposed one-bit FA/FS.

We have implemented a new FA/FS circuit in QCA simulation tools. We have used the multi-layer wire crossing to design an efficient QCA FA/FS, in which cell count, area and latency are less than previous design. Fig. 5 depicts a layout for one-bit FA/FS by QCAdesigner as a popular simulation tool.

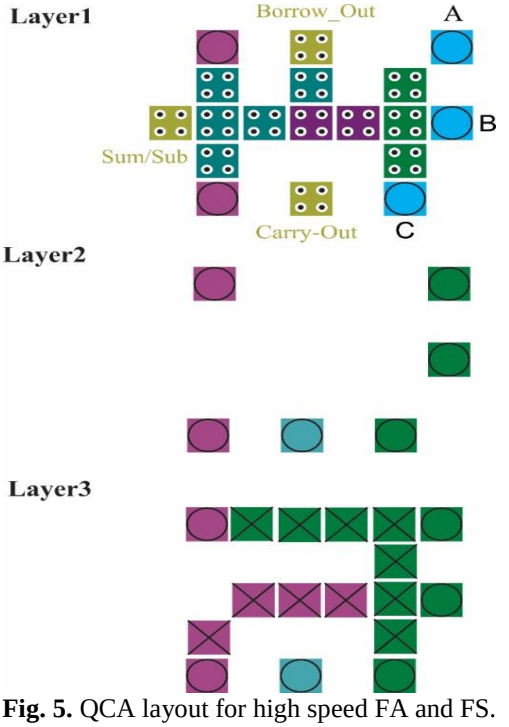

Fig. 5. QCA layout for high speed FA and FS.

4. SIMULATION RESULT

The functionality of the proposed design is evaluated by QCA designer version 2.0.3 based on coherence vector and bistable approximation simulation engine which its parameters are depicted in Table 2 and Table 3.

Table 2. Coherence vector applied parameters.

Parameter	Value	
Temperature	1.000000	K
Relaxation time	4.1356675e-14	s
Time Step	1.000000e-016	s
Total Simulation Time	7.000000e-011	s
Clock High	9.800000e-022	J
Clock Low	3.800000e-023	J
Clock shift	0.000000e+000	
Clock Amplitude Factor	2.000000	
Radius of Effect	80.000000	nm
Relative Permittivity	12.900000	
Layer Separation	11.500000 nm	

Table 3. Bistable approximation applied parameters.

Parameter	Value	
Number of samples	50000	
Convergence tolerance	0.001000	
Radius of effect	65.000000	nm
Relative permittivity	12.900000	
Clock low	3.800000e-023	J
Clock high	9.800000e-022	J
Clock shift	0	
Clock amplitude factor	2.000000	
Layer separation	11.500000	
Maximum iterations per sample	100	

As it is shown in Fig. 6, the simulation results indicate that the proposed circuit works properly. Comparison of the results between the proposed circuit and previous design are reported in Table. 4. The comparison of the result demonstrates that our proposed design is better than other presented circuits in term of the cell count, area and number of majority gates. Delay of our circuit is equal to pervious work that is introduced by [8].

Reducing the number of majority gates influences the power dissipation. QCApro tools can not measure the power dissipation of circuits that are designed in multilayers. Consequently, we are not able to compute the exact mentioned quantities [17].

We have investigated variation of temperature on outputs polarization. QCADesigner tools can help to change the temperature by enhancing this parameter in coherence vector engine option. According to the Fig.

7, we observe that polarization of outputs is reduced if the temperature is increased.

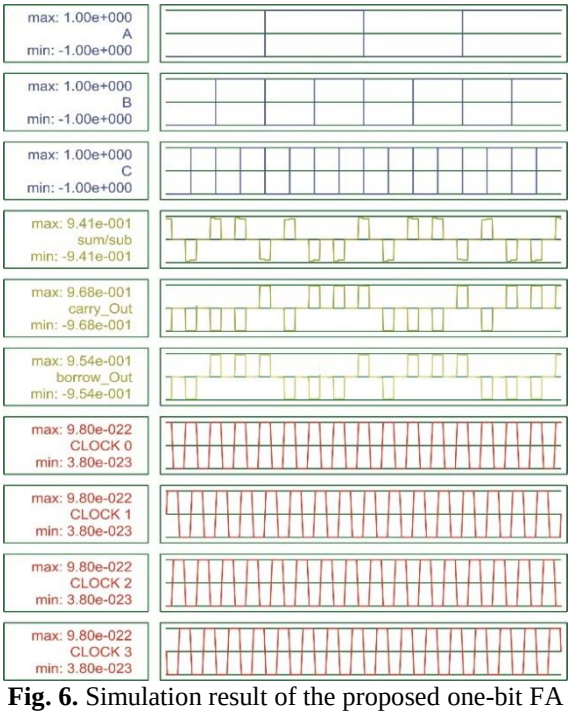

Fig. 6. Simulation result of the proposed one-bit FA and FS.

Table 4. Comparison results.

Proposed circuit	Complexity (cell)	Circuit area (μm^2)	Delay (clock cycle)
Proposed	43	0.01	0.5
[12]	53	0.039	0.5
[11]	180	0.19	1.75

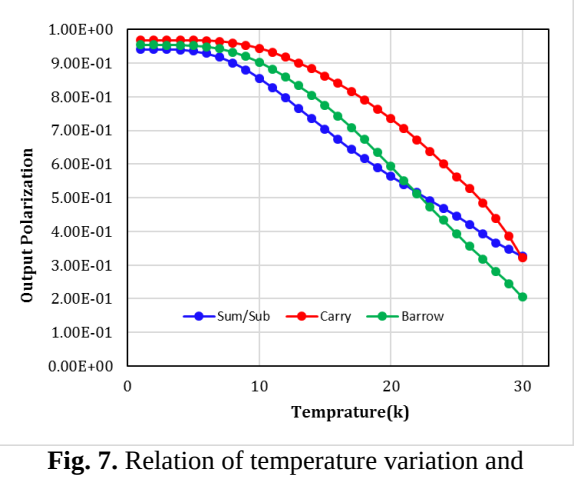

Fig. 7. Relation of temperature variation and polarization of output for the proposed Fa/Fs.

5. CONCLUSIONS

In this paper, we proposed a novel design of one-bit Fulladder/Full subtractor cell for Quantum-dot cellular automata. The layouts and functionality, that is checked by QCADesigner, demonstrated that the proposed circuit is more efficient than the previous designs in terms of cell counts and complexity. Compared to the best state-of –the art technology, our proposed FA/FS cell benefits from 19% to 20% improvement in terms of cell counts compared to the best work studied in the literature. Furthermore, temperature analysis of the proposed design demonstrated that our circuit is more robust than the other previous works. According to the simulation results, we concluded that this new design is suitable for larger arithmetic QCA circuits studied in the previous work.

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