Asymmetrical Modular Multilevel Converter (A-MMC) with Mixed Cell Sub-Modules (SM) for Improved DC Fault Blocking Capability and Reduced Component Count

Himanshu N. Chaudhari[1*], Pranav B. Darji[2]
1- Department of Electrical Engineering, SVNIT, Surat, India.
Email: d18el002@eed.svnit.ac.in (Corresponding author)
2- Department of Electrical Engineering, SVNIT, Surat, India.
Email: pranav@eed.svnit.ac.in

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ABSTRACT:
In this article, asymmetrical modular multilevel converter (A-MMC) topology using mixed cell (SM) with DC-side fault blocking capability and the reduced component count is proposed. The mixed cell submodule is made up of a full-bridge (FB-SM) and a half-bridge (HB-SM) with asymmetric capacitor voltage based on geometric propagation (GP) ratio. Each mixed cell submodule can generate a maximum of four output voltage levels with binary GP ratio and five output voltage levels with ternary GP ratio using six controlled switches and two asymmetric capacitors. The proposed A-MMC topology requires nearly half the number of components and voltage sensors compared to conventional topologies. This will result in simpler control structure of A-MMC with DC fault blocking capability. A voltage balancing algorithm based on normalization is used for capacitor voltage balancing and a hybrid pulse width modulation (H-PWM) technique to generate gating signals. Detailed operational concepts of the proposed topology, the pre-charging process of a capacitor, and performance with different modulation indexes are discussed in length. A detailed simulation model of A-MMC under different operating conditions is carried out using MATLAB/SIMULINK environment. To show the benefits of mixed cell SM, a comparison between the proposed mixed cell and other existing cells is presented in detail. The simulation results analysis show effectiveness of proposed schemes over other schemes presented in literature.

KEYWORDS: Asymmetrical Modular Multilevel Converter (A-MMC), HVDC System, Mixed Cell, Hybrid Modulation Technique, Reduced Component Count, DC Fault Blocking Capability.

1. INTRODUCTION

The modular multilevel converter is used in various types of power applications because of its modular structure, scalability, higher productivity, and small size input capacitor compared to multilevel inverters. MMC is used in numerous applications, like flexible alternating current transmission systems (FACTs) [1], high voltage direct current systems [2], electric drives [3], and renewable energy systems [4]. However, due to its unique modular structure, MMC still has many problems to be solved in terms of DC side fault control [5], capacitor voltage balancing, a higher number of component requirements, etc. The submodules based on half-bridge (HB-SM) are used as the main configuration in MMC [6]. However, a half-bridge submodule-based MMC (HB-MMC) is unable to block the fault that occurs on the DC side. Asymmetrical HB-SM based MMC was proposed in [7]. This topology required least number of switching devices to generate higher output voltage levels but does not possess DC fault handling capability. To handle the DC faults, a submodule based on full-bridge (FB-SM) was proposed to possess DC fault blocking capability. Though, the number of control switches is twice in FB-SM as equated to HB-SM. The costs of MMC increases, also there is a higher power loss because in each submodule the current flows through two control switches alternately one as in an HB-SM. In [8,9,10], three level Sub-module with DC fault blocking capability was proposed but it requires higher switching devices.

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To solve the above-mentioned issues this article proposes an asymmetrical approach with mixed-cell [12] based modular multilevel converter topology which is having series-connected submodules in each arm comprised of a full-bridge and a half-bridge connected in a cascade having an asymmetrical capacitor voltage ratio of 1:2 (binary) and 1:3 (ternary) across the floating capacitors. The half-bridge in the sub-module allows for utilization of the advantage of more output levels with a smaller number of switches hence a smaller number of floating capacitors and voltage sensors are required. Also, a full bridge in a sub-module provides DC fault handling capability. It is also possible for A-MMC to deal with low DC voltage operation, DC short circuit fault ride through, and the black starting [14] hence the reliability can be enhanced by connecting several modules in series.

A combination of phase-shifted and level-shifted PWM called a hybrid modulation technique is used to generate gating signals for control switches to obtain different voltage levels, utilizing an SM of the A-MMC. A modified voltage balancing algorithm, where the output voltages of the full-bridge and half-bridge of each sub-module are measured using voltage sensors and normalized then sorted to aid in voltage balancing [7,13]. This voltage balancing algorithm improves performance by reducing the capacitor voltage ripple compared to the conventional voltage balancing algorithm. A **3-ϕ** A-MMC having two SMs in each arm is simulated using MATLAB-Simulink to generate a maximum 13- level output voltage using binary GP ratio and 17- level output voltage waveform using ternary GP ratio. Detailed simulation results are illustrated which show the figure of the output currents and voltages with or without interleaving angle. A comparison of A-MMC with conventional MMC having the same number of output voltage levels is also shown to illustrate the additional advantages of such A-MMCs.

The remainder of this article is organized as follows. Section II introduces the mixed cell sub-module-based A-MMC topology and describes the circuit and its working. The hybrid modulation technique, and modified VB algorithm, are summarized in Section III. In Section IV, the flow chart for the pre-charging process of capacitors for binary GP and ternary GP ratio is discussed. Simulation results by considering two modules per arm and a comparison of the proposed topology with conventional MMCs is described in section V and the article concludes in Section VI.

2. MIXED CELL SUBMODULE-BASED A-MMC TOPOLOGY AND ITS OPERATION

The proposed topology illustrated here in this article allows using novel asymmetric mixed-cell with traditional MMC topology. A 3-ϕ structure of the proposed converter topology is shown in Fig.1. Each leg comprises two arms in the A-MMC, having *n* series-connected cells in both arms, and by appropriate switching of the cells required output voltage can be generated. Consider A phase, for example, the relationship among ac voltage, dc voltage, and arm voltage is shown as (1) [7], where V_{au} and V_{al} are the upper and down arm sub-modules output voltage, V_a is the A-phase voltage, V_{dc} is the DC bus voltage and V_{dc-} and V_{dc+} are the negative and positive phase to ground voltage.

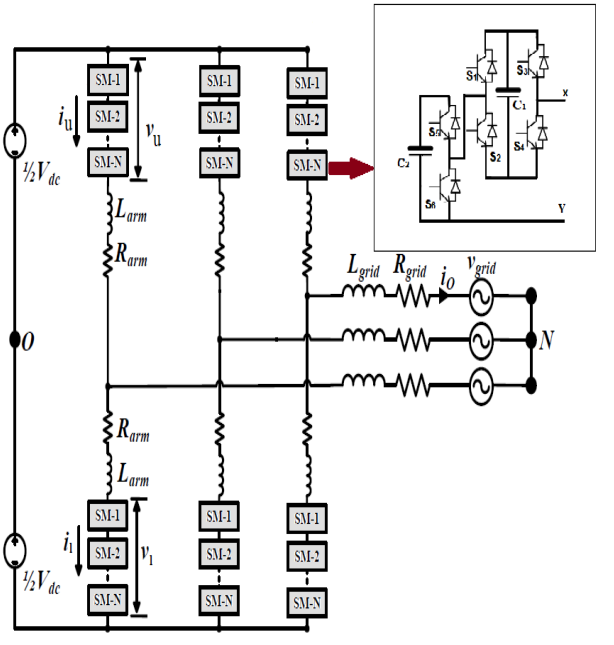


Fig. 1. Circuit configuration of Mixed cell SM-based A-MMC.

$$v_{au} = 0.5V_{dc} - v_a - L\frac{di_{au}}{dt}$$

$$v_{al} = 0.5V_{dc} + v_a - L\frac{di_{al}}{dt} \quad (1)$$

$$V_{dc+} = |V_{dc-}|$$

The relationship among arm current, AC, and DC is illustrated as,

$$i_a = i_{au} - i_{al}$$

$$i_{dc} = i_{au} + i_{bu} + i_{cu} \quad (2)$$

The internal architecture of the mixed cell is also shown in Fig. 1. The cell consists of a half-bridge and a full bridge connected in series, each having a capacitor with an asymmetric capacitor voltage rating. The control

switches of half-bridge (S_5 and S_6) are rated for V_C voltage, and the control switches of full-bridge (S_1, S_2, S_3, and S_4) in a cell are rated at a voltage of $2V_C$ for binary. And for ternary control switches of half-bridge (S_5 and S_6) are rated for $3V_C$ voltage, and the control switches of full-bridge (S_1, S_2, S_3, and S_4) in a cell are rated at a voltage of V_C. This is compared to traditional MMCs which consists of symmetric cells with equal capacitor voltage rating. By giving proper gating signals to the control switches, the output voltage of a cell can reach four output voltage levels (0, V_C, $2V_C$, $3V_C$) for binary as per equation (3) and five output voltage levels (0, V_C, $2V_C$, $3V_C$, $4Vc$) for ternary as per equation (4). The DC-link voltage V_{dc} can be related to cell capacitor voltage by (3-4).

$$\overline{v_{XY}} = S_1.S_4\,2V_c + S_5.V_c$$

$$n.V_c + n.2V_c = V_{dc} \Rightarrow V_c = \frac{V_{dc}}{3n} \quad (3)$$

$$\overline{v_{XY}} = S_1.S_4.V_c + S_5.3V_c$$

$$n.V_c + n.3V_c = V_{dc} \Rightarrow V_c = \frac{V_{dc}}{4n} \quad (4)$$

Table 1. Switching states for a sub-module with binary GP.

V_{xy}	S_1	S_2	S_3	S_4	S_5	S_6	i	V_{c1}	V_{c2}
0	1	0	1	0	0	1	≥ 0 OR <0	=	=
	0	1	0	1	0	1			
Vc	1	0	1	0	1	0	≥ 0	↑	=
							<0	↓	
	0	1	0	1	1	0	≥ 0	↑	
							<0	↓	
2Vc	0	1	1	0	0	1	≥ 0	=	↑
							<0		↓
3Vc	0	1	1	0	1	0	≥ 0	↑	↑
							<0	↓	↓
−Vc	1	0	0	1	1	0	≥ 0	↑	↓
							<0	↓	↑
−2Vc	1	0	0	1	0	1	≥ 0	=	↓
							<0	=	↑

Switches S_1 –S_6 contain IGBT and reverse connected diodes, and ↑, ↓ and = indicates states of charge of the cell capacitors (discharge, charge, and unchanged) for the distinct polarity of arm current

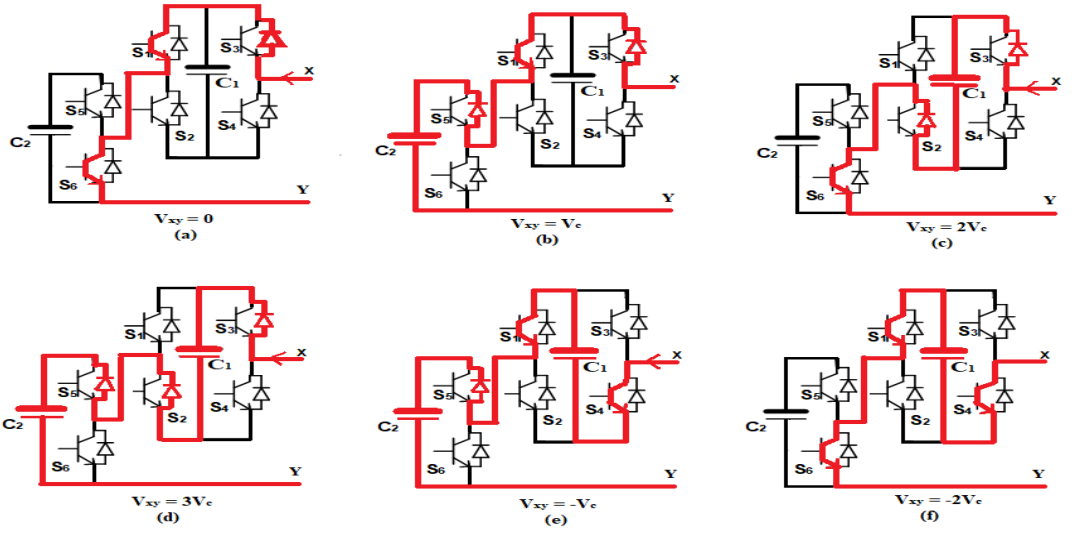


Fig. 2. Current paths of mixed cell sub-module based A-MMC with binary GP ratio, switching states. (a) $V_{xy} = 0$. (b) $V_{xy} = V_c$. (c) $V_{xy} = 2V_c$. (d) $V_{xy} = 3V_c$. (e) $V_{xy} = -V_c$. (f) $V_{xy} = -2V_c$.

The switching states of control switches and generation of cell output voltage levels are given in Table 1 using binary GP ratio between capacitor voltage of a cell. For the same, Fig. 2 shows the different states considering a positive current direction. The proposed configuration permits a cell to generate six different output voltage levels: 0, V_C, $2V_C$, $3V_C$, - V_C, -$2V_C$ using binary GP ratio between capacitor voltage of a submodule.

Table 2 shows the switching states of control switches and generation of cell output voltage levels based on the ternary GP ratio between capacitor voltage of a submodule. The proposed configuration allows a sub-module to generate 6 distinct voltage levels: 0, V_C, $2V_C$, $3V_C$, $4V_C$, - V_C.

Table 2. Switching states for a sub-module with ternary GP.

V_{xy}	S_1	S_2	S_3	S_4	S_5	S_6	i	V_{c1}	V_{c2}
0	1	0	1	0	0	1	≥0 OR <0	=	=
	0	1	0	1	0	1			
Vc	0	1	1	0	0	1	≥0	=	↑
							<0		↓
2Vc	1	0	0	1	1	0	≥0	↑	↓
							<0	↓	↑
3Vc	1	0	1	0	1	0	≥0	↑	=
							<0	↓	
	0	1	0	1	1	0	≥0	↑	
							<0	↓	
4Vc	0	1	1	0	1	0	≥0	↑	↑
							<0	↓	↓
−Vc	1	0	0	1	0	1	≥0	=	↓
							<0		↑

Switches S1 –S6 contain IGBT and reverse connected diodes, and ↑, ↓ and = indicates states of charge of the cell capacitors (discharge, charge, and unchanged) for the distinct polarity of arm current.

The proposed topology minimizes the requirement of voltage sensors up to 50% compared to conventional topologies and it possesses DC fault handling capability which eliminates the need of DC fault control devices. Also, the proposed sub module topology is able to generate higher number of output voltage levels leading to reduction in THD. Due to proposed A-MMC topology, to generate same output voltage levels number of sub module requirement is reduced that will lead to reduction in overall IGBT requirement as well as reduces gate driver requirement for switching devices.

3. MODULATION AND CONTROL OF A-MMC

In this article, in each submodule of the A-MMC, there is a capacitor voltage asymmetry. Since they are made from a series connection of a half-bridge and a full bridge, one at V_C volts and the other at *2Vc or 3Vc* volts. It generates maximum of four or five output voltage levels in A-MMC as per the GP ratio between the capacitor voltage of a submodule.

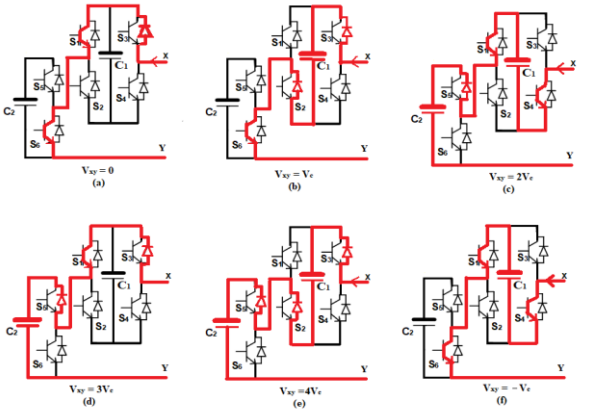
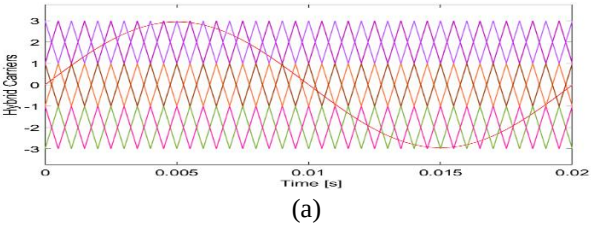


Fig. 3. Current paths of mixed cell sub-module with ternary GP ratio, switching states. (a) $V_{xy} = 0$. (b) $V_{xy} = V_c$ (c)$V_{xy} = 2V_c$ (d)$V_{xy}=3V_c$ (e) $V_{xy} = 4V_c$. (f) $V_{xy} = -V_c$.

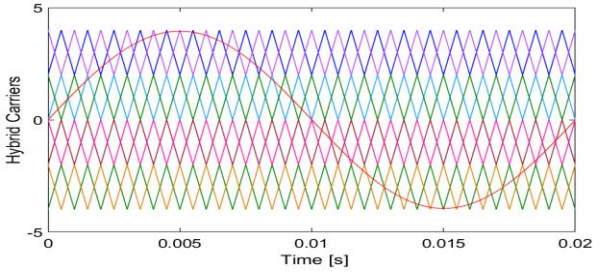
A combination of level-shifted pulse width modulation and phase-shifted modulation called the hybrid PWM technique is used for A-MMC [7]. In Hybrid PWM, in the context of a single mixed cell submodule with binary GP ratio between capacitor voltage of a submodule, a group of three level-shifted carriers are first stacked on top of one another and three phase-shifted triangular carriers come into play. Hybrid PWM can also be utilized with carrier interleaving as equation (5) [7], with the A-MMC to obtain higher output voltage levels.

$$\theta = \begin{cases} 0, & \text{for odd n} \\ \dfrac{\pi}{n}, & \text{for even n} \end{cases} \tag{5}$$

In this article, two sub-modules in each arm are used to construct an A-MMC and driven by the Hybrid PWM technique. For A-MMC based on binary GP ratio, there are three groups of stacked carriers while for ternary GP ratio four groups of stacked carriers are used. For each phase of the A-MMC, these hybrid triangular carriers are compared with v^{*u} (upper arm) and v^{*l} (lower arm), two normalized sinusoidal references to synthesize the output voltage. Pulses are then generated, corresponding to each submodule in the entire phase-leg. These pulses are then passed through the digital decoder logic, to generate individual pulses for the submodules.



(a)



(b)

Fig. 4. Hybrid Modulation technique for a submodule based on (a) Binary GP ratio [7] (b) Ternary GP ratio.

The voltage balancing technique based on normalization has been developed here for A-MMC based on the ternary GP ratio of the capacitor voltage of a submodule. This normalization is done as per equation (6), where V_C and 2Vc (Binary GP), and as per equation (7), where Vc and 3Vc (Ternary GP) are the intended voltage values.

$$v'_{c1} = v_{c1} / V_c$$

$$v'_{c2} = v_{c2} / 2V_c \quad (6)$$

$$v'_{c1} = v_{c1} / V_c$$

$$v'_{c2} = v_{c2} / 3V_c \quad (7)$$

The decision of which submodule to insert/remove is done once the normalized values are computed and it depends on the direct current flow [20]. Using the realization of the direction of then, the capacitor which is farthest from the normalized rated value is selected. The modulation will demand only one level to be inserted/removed at a time. Thus, as a case, the addition of a voltage level in an arm can be done according to the voltage balancing algorithm based on normalization for binary GP in Fig. 5 [7], and the algorithm is shown in Fig. 6 for the ternary GP ratio of capacitor voltage in a cell.

4. PRE-CHARGING OF A CAPACITOR

To pre-charge the submodule capacitors to appropriate V_C and $2V_C$ voltage levels with binary GP ratio and V_C and $3V_C$ voltage levels with ternary GP ratio PWM technique are used. During the pre-charge time, a resistor connected in series is used in a DC-bus path to keep the charging current low and it can be bypassed with a circuit breaker after the pre-charge process is complete. Based on the RC time constant capacitors voltage slowly increases and hence all the capacitor starts to get charged. The voltage sensors keep a check on the capacitor voltages and give input to a controller. As soon as the capacitors of each cell reach the reference voltage value a controller restricts the gate pulses to the cell. To prevent the load current, identical number of cells must be inserted during the whole pre-charge process. The whole pre-charge process for A-MMC is developed here which act follows the flowchart shown in Fig. 7.

5. SIMULATION MODELS AND THEIR ESULTS

The 3-phase A-MMC with mixed cell submodule was simulated in MATLAB/Simulink having four sub-modules per phase. Table 2 illustrates the parameters used for the simulation. Simulation results of the proposed A-MMC are discussed in detail here in this section.

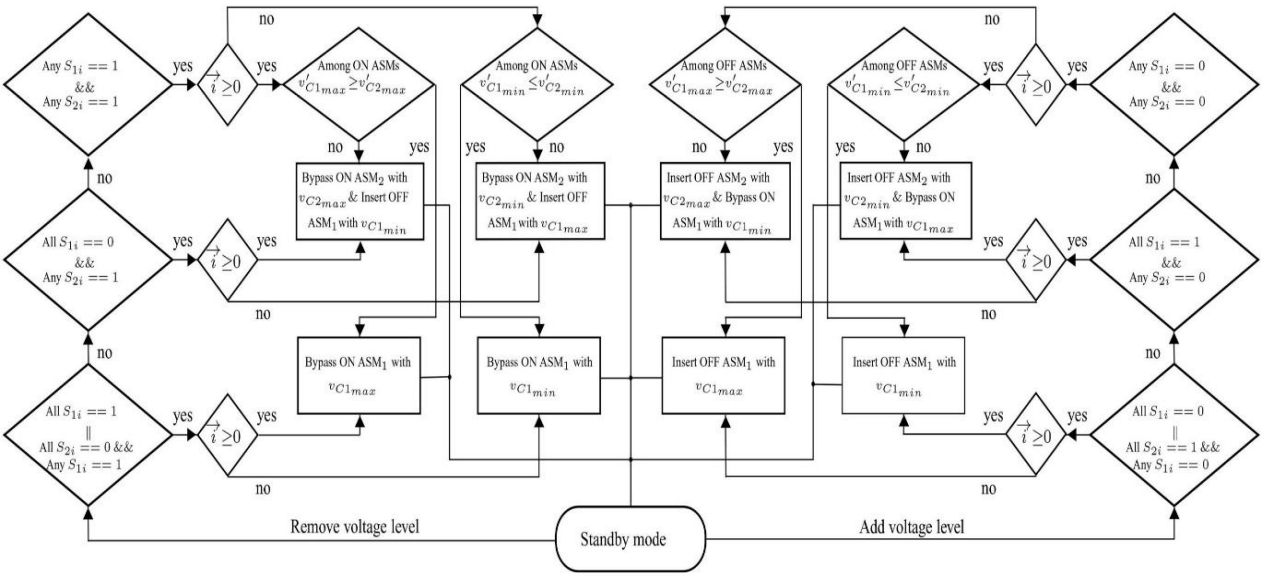


Fig. 5. Modified Voltage balancing (VB) algorithm (for Binary GP ratio of capacitor voltage in a submodule) [7].

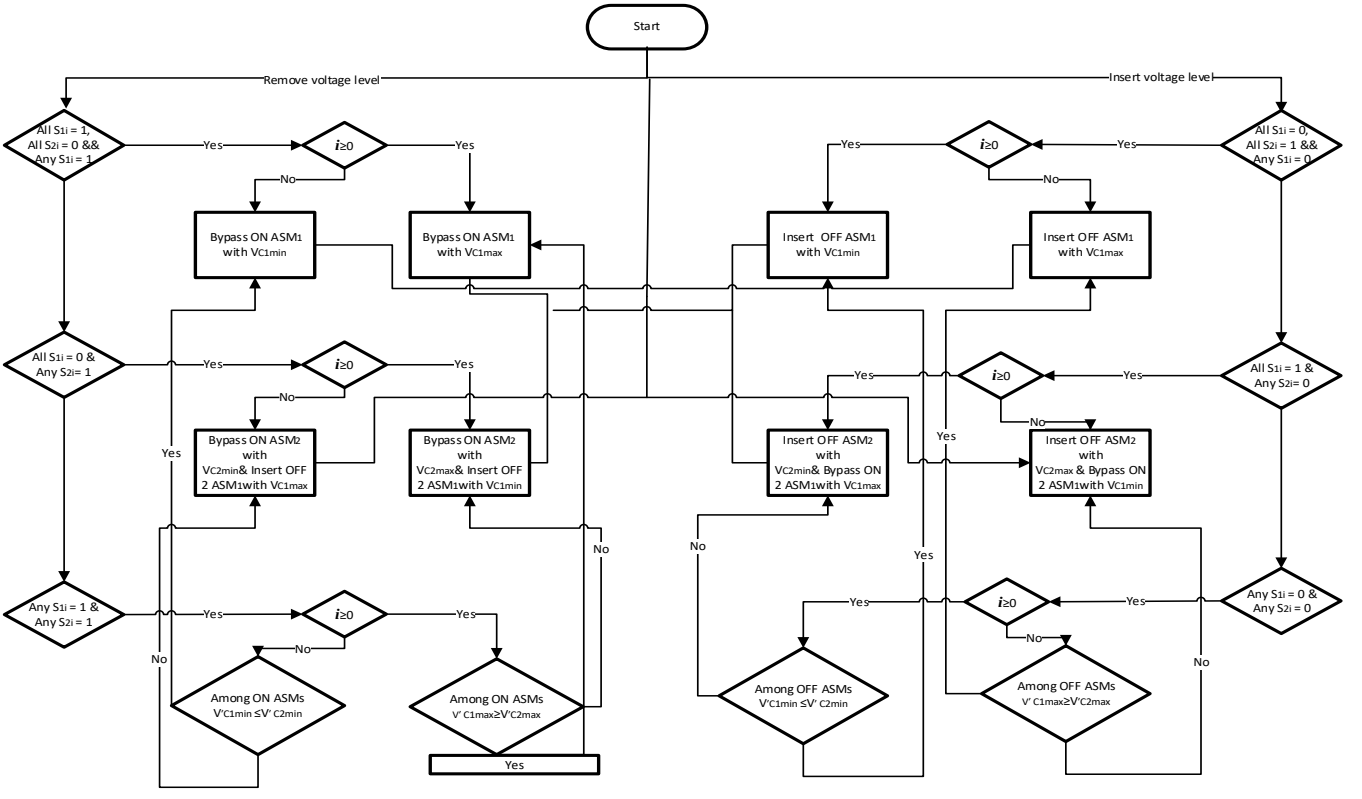


Fig. 6. Modified Voltage balancing (VB) algorithm (for Ternary GP ratio of capacitor voltage in a submodule).

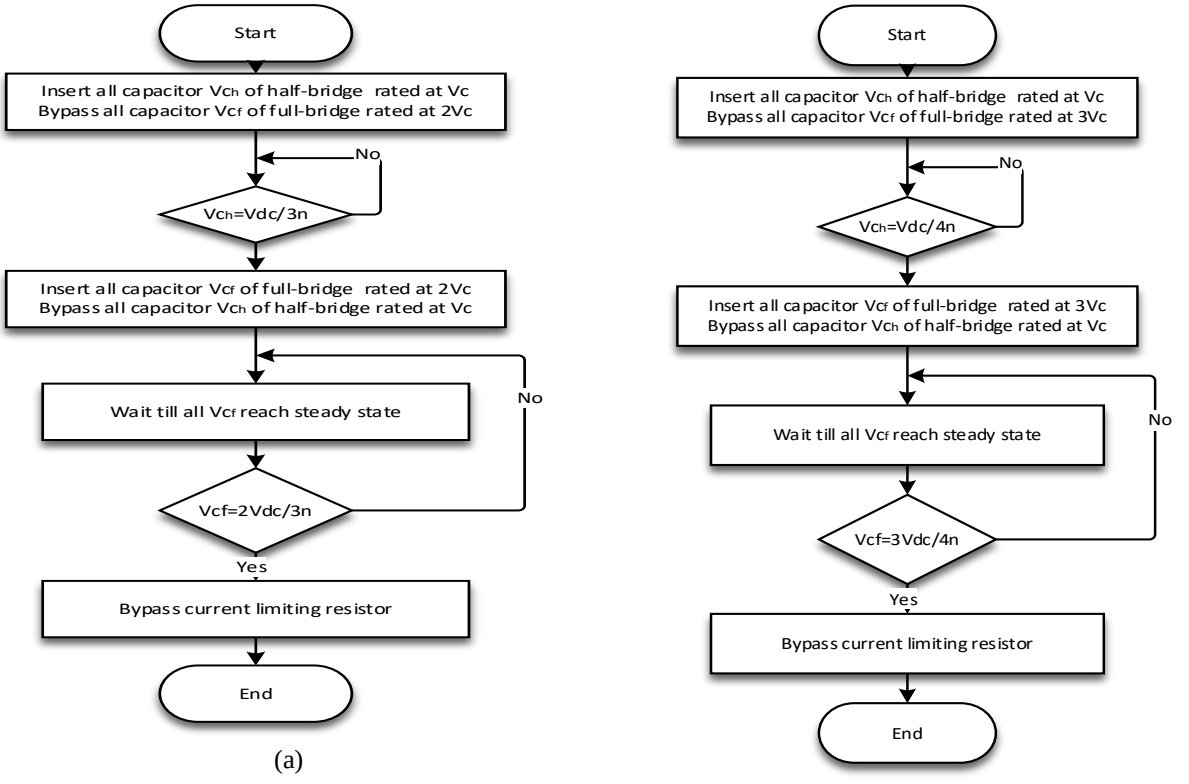


Fig. 7. Flow-chart for a pre-charge process of the capacitors (a) Binary GP ratio [7] (b) Ternary GP ratio.

For a 9 kV DC bus, the individual capacitor voltage rating with binary GP ratio is 1500 V and 3000 V for half-bridge and full-bridge, respectively as derived from (3) while for ternary GP ratio of capacitor voltages are 1125 V for full-bridge and 3375V for half-bridge, respectively. The capacitor selection must be done such that the actual capacitance ensures the constant of the proposed A-MMC concerning a traditional MMC for an equal number of output voltage levels. A proposed A-MMC has two pairs of capacitors having an actual capacitance of C/3 and 2C/3 for binary GP ratio and C/4 and 3C/4 for ternary GP ratio, respectively, in each arm. Assuming $C_2 = 1.5*C_1$ to do charge balance, compared to capacitance C per cell of the traditional MMC, the A-MMC requires 5C/9 for half-bridge and 5C/6 for full-bridge for the binary GP ratio, respectively. Therefore, concerning to 10 mF of capacitance required in each cell of the traditional MMC, the proposed structure of A-MMC requires 5.55nF and 8.33 mF capacitance, respectively for the binary GP ratio.

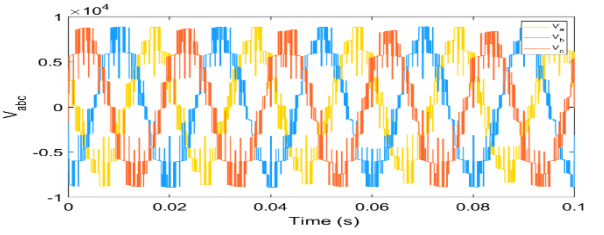
An A-MMC can generate a maximum thirteen-level output voltage per phase without carrier interleaving and twenty-five-level output voltage per phase with carrier interleaving, using two mixed cell submodules in an arm. It requires a total of twelve IGBTs and diodes per arm, two capacitors of *Vc* voltage, and two of *2Vc* voltages for binary GP ratio.

In A-MMC, it is possible to obtain a higher number of output voltages levels using the same number of cells with using an interleaving angle in the hybrid modulation technique. Hybrid PWM can also be deployed with similar carrier interleaving, with the A-MMC using binary GP ratio, to generate 3n + 1 to 6n + 1 output voltage levels and 4n+1 to 8n+1 output voltage levels with ternary GP ratio.

Table 3. Simulation parameters.

Parameters	A-MMC
Submodules/phase	2
Output frequency	50 Hz
Switching frequency (f_s)	1 kHz
Arm resistor R_a	0.1 Ohm
Arm inductor L_a	1 µH
DC bus voltage V_{dc}	9 kV
Submodule capacitor C_1	5.66 mF
Submodule capacitor C_2	8.33 mF
Modulation technique	Hybrid PWM

The first set of simulation results are shown in Fig. 8 as (a&b) shows the 13-level output voltage, and output current with having THD of 20.23% and 6.28% respectively using a hybrid modulation technique without interleaving angle and having two submodules per arm. Fig. 8 (c) shows the capacitor voltages of SMs which are balanced at voltage 2Vc. Similarly, Fig. 8 (d) shows that the capacitor voltages of SMs are balanced at Vc, this is observed in the capacitor with Vc voltages in an SM having higher ripple content than capacitors with 2Vc voltage.



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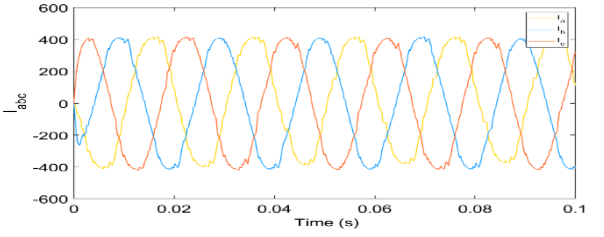

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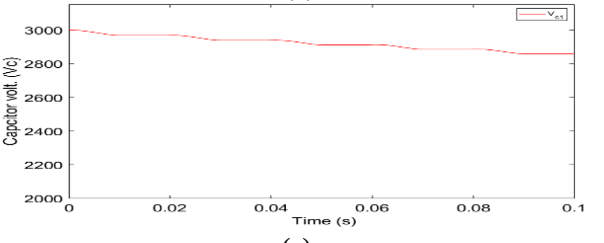

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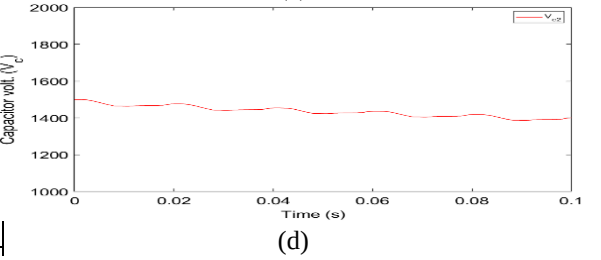

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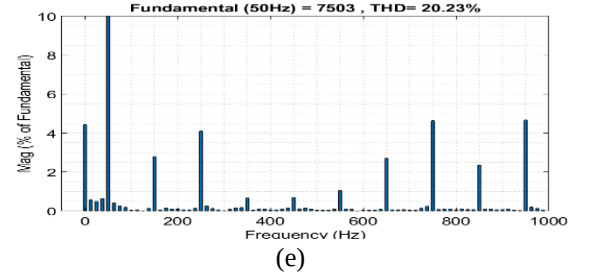

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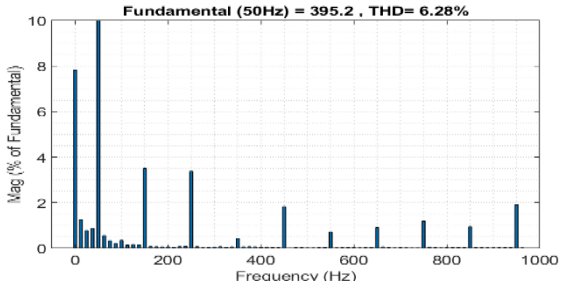
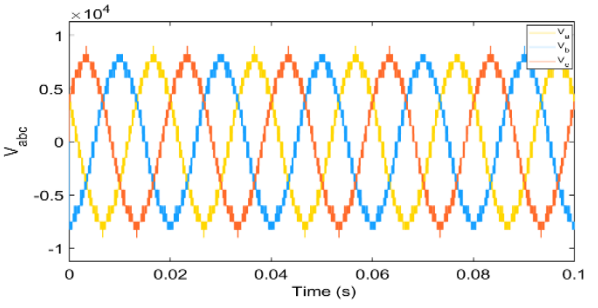


(f)

Fig. 8. Simulation results of mixed cell submodule based A-MMC with binary GP ratio and without carrier interleaving (a) O/p voltage V_{abc} (b) O/p current I_{abc} (c) C_1 voltage (d) C_2 voltage (e) O/p voltage THD (f) O/p current THD .



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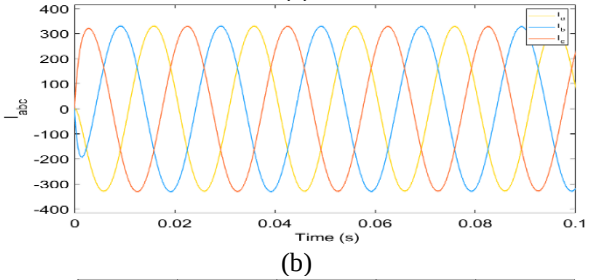

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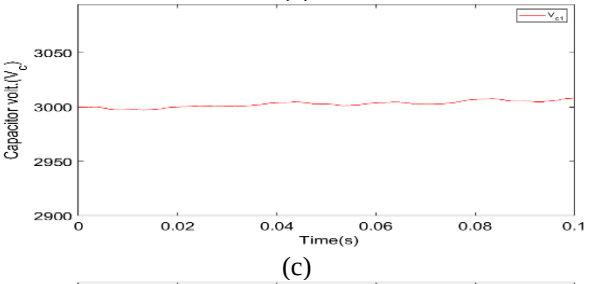

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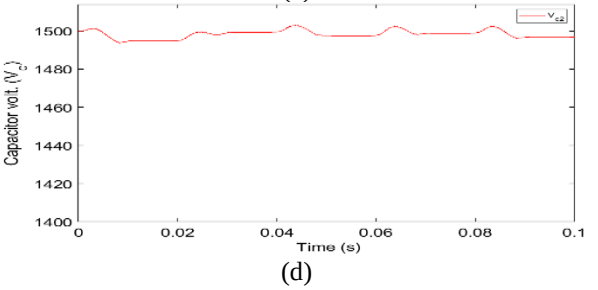
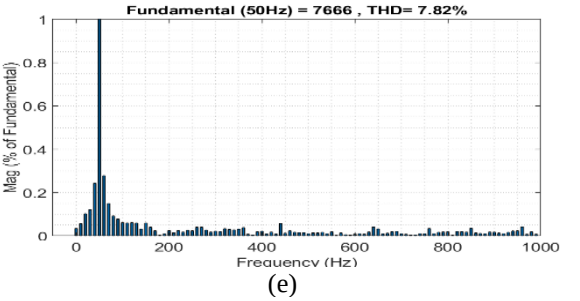
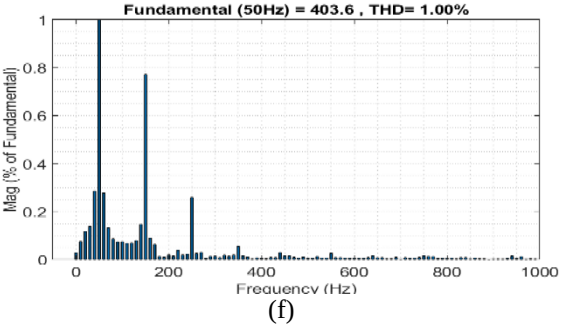


(d)

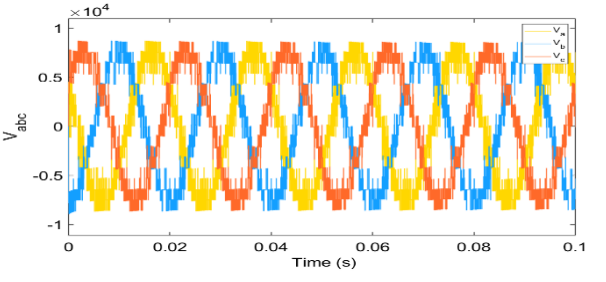


(e)

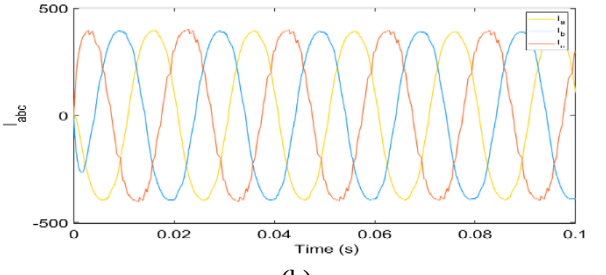


(f)

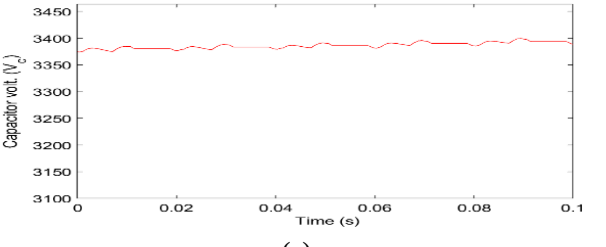
Fig. 9. Simulation results of mixed cell submodule based A-MMC with binary GP ratio and with carrier interleaving O/p voltage V_{abc} (b) O/p current I_{abc} (c) C_1 voltage (d) C_2 voltage (e) O/p voltage THD (f) O/p current THD.



(a)



(b)



(c)

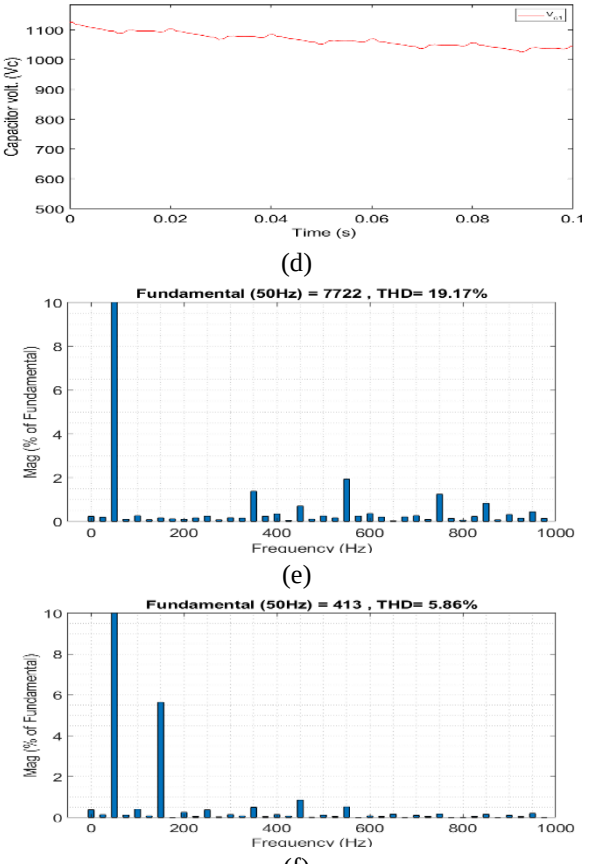
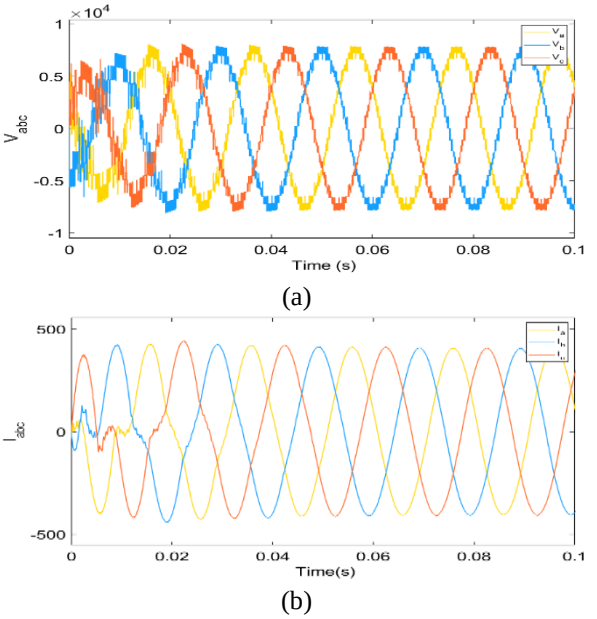


Fig. 10. Simulation results of mixed cell submodule based A-MMC with ternary GP ratio and without carrier interleaving (a) O/p voltage V_{abc} (b) O/p current I_{abc} (c) C_1 voltage (d) C_2 voltage(e) O/p voltage THD (f) O/p current THD **.**



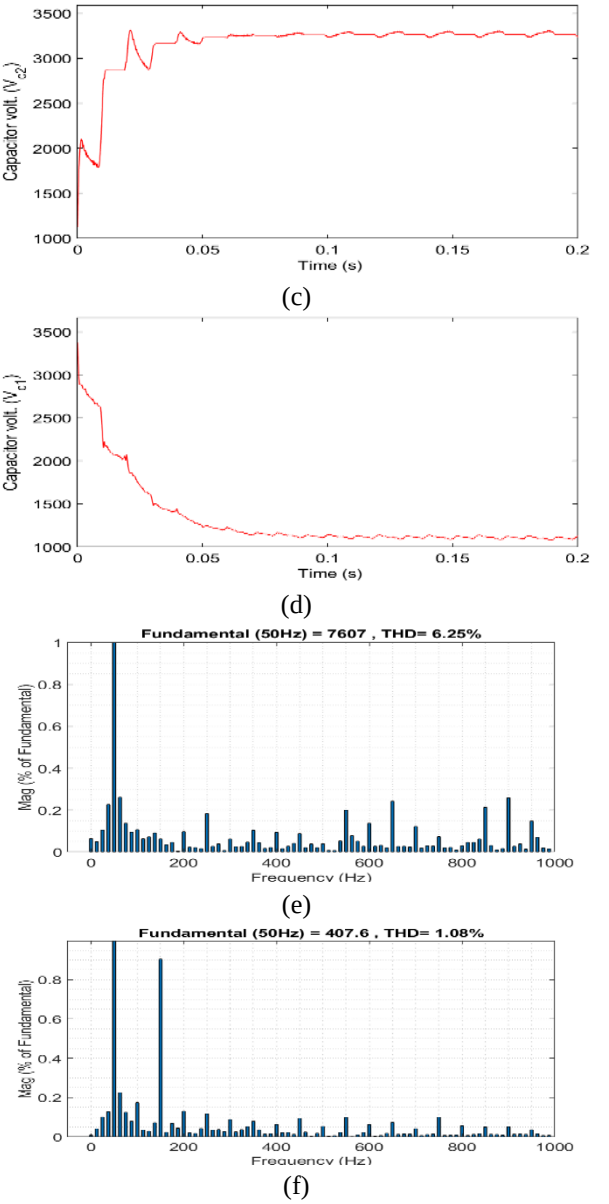
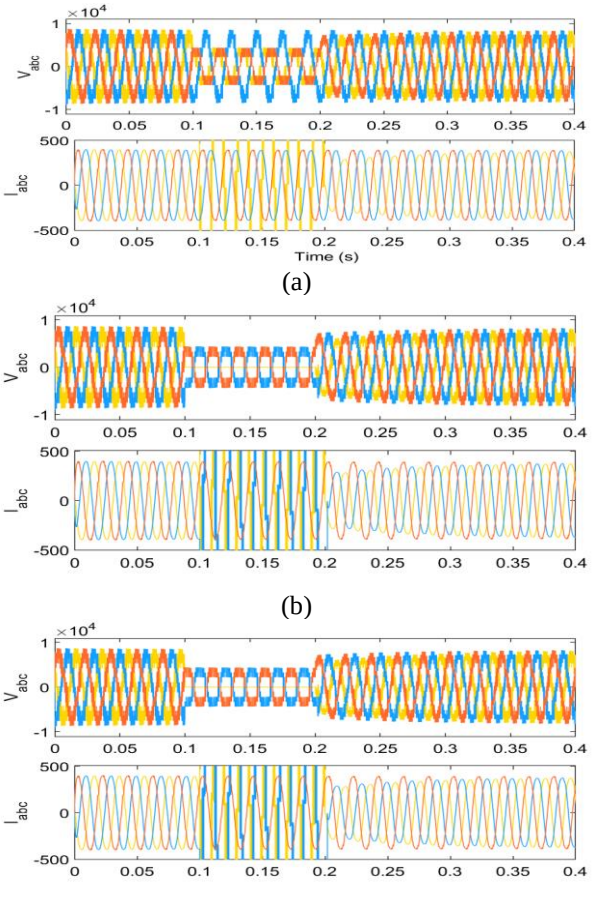


Fig. 11. Simulation results of mixed cell submodule based A-MMC with ternary GP ratio and with carrier interleaving (a) O/p voltage V_{abc} (b) O/p current I_{abc} (c) C_1 voltage (d) C_2 voltage (e) O/p voltage THD (f) O/p current THD.

Fig. 9 shows the 25-level output voltage with THD 7.82%, output current with THD 1.00%, capacitor voltage, and harmonic spectrum of output voltage and current using a hybrid modulation technique with an interleaving angle with having the same number of submodules per arm. From the above-illustrated figure the capacitor voltage ripples are less and within the permissible limit. In Fig. 10 the 17-level output voltage with THD 19.17%, output current with THD 5.86%, capacitors voltage, and the harmonic spectrum of phase

voltage and current using a hybrid modulation technique without interleaving angle with two submodules per arm are shown. Fig, 11 shows the 33-level output voltage with THD 6.25%, output current with THD 1.08%, capacitors voltage, and the harmonic spectrum of phase voltage using a hybrid modulation technique with an interleaving angle with the same number of submodules per arm. The output voltage and output current synthesized have very low THD content in mixed cell SM-based A-MMC with binary GP ratio using carrier interleaving compared to without carrier interleaving.



(a)

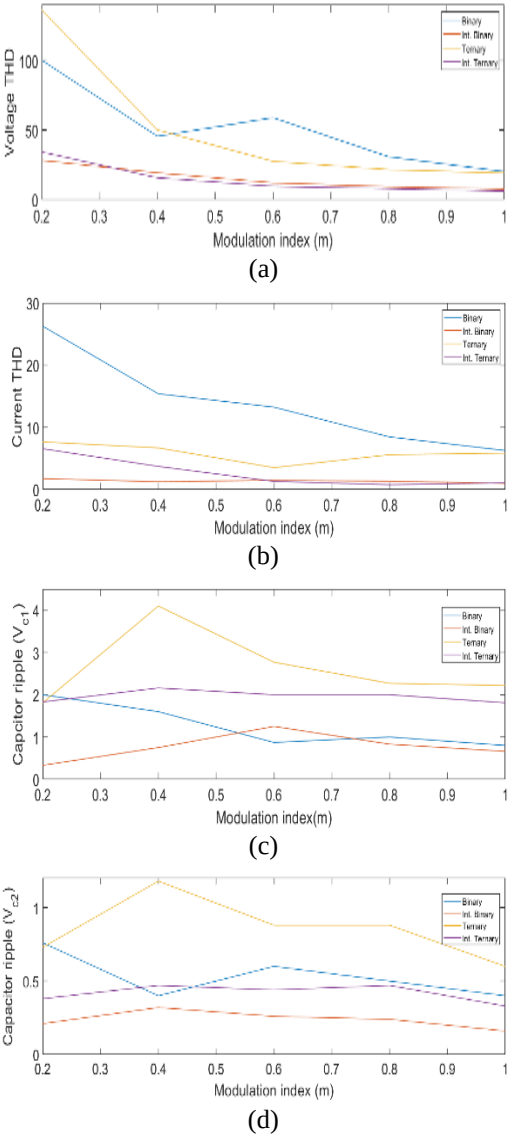
(b)

(c)

Fig. 12. Simulation results of A-MMC under (a) line-to-ground (L-G) fault, (b) line-to-line-to-ground (L-L-G) fault, and (c) line-to-line-to-line ground (L-L-L-G) fault.

To check the dynamic performance and the efficacy of the modified voltage balancing algorithm, various faults like L-G, L-L-G, and L-L-L-G are applied from 0.1 s to 0.2 s to both the configuration of A-MMC. The L-G fault is applied at t=0.1 second to 0.2 seconds as in figure 12(a) and the system gets stabilized within 4-5 cycles after the fault is removed. Fig. 12 (b) shows that when the L-L-G fault is applied the balancing algorithm works satisfactorily but it requires 6-7 cycles to get stabilized. As can be seen in Fig. 12 (c), after L-L-L-G faults the system recovers faster than the above-mentioned fault conditions. These results verify the performance of A-MMC with a newly developed voltage balancing (VB) newly developed block. Hence, from the above, it is said that the newly developed VB block is performing better under abnormal conditions.

A comparison of THD in output voltages and currents is illustrated. Fig. 13 a and b show the THD in output voltage and current as a function of the modulation index. From that, it is verified as the modulation index increases, THD decreases, and capacitor ripples are also within permissible limits.



(a)

(b)

(c)

(d)

Fig. 13. Variation with modulation index (m) of (a) O/P voltage THD, (b) O/P current THD, (c) Capacitor voltage ripple of V_{c1}, (d) capacitor voltage ripple of V_{c2}.

Table 4. Comparison of A-MMC with other topologies.

Parameters	Types of modules						
	Half-bridge (HB) [22]	Full-bridge (FB) [22]	Asymmetrical Half-bridge (A-HB) [7,13]	Asymmetrical Hybrid SM (A- HB FB)		Asymmetrical Full-Bridge (A-FB)	
				Binary GP	Ternary GP	Binary GP	Ternary GP
No. of submodule*	2. n	2. n	0.66 n	0.66 n	0.5 n	0.66 n	0.5 n
No. of IGBT's	4.n	8.n	2.64 n	3.96 n	3. n	5.38 n	4. n
No. of diodes	4. n	8. n	2.64 n	3.96 n	3. n	5.38 n	4. n
No. of SCR	2. n	0	1.32 n	0.66 n	0.66 n	0	0
No. of a Bypass switch	2. n	2. n	1.32 n	1.32 n	1.0 n	1.32 n	1.0 n
No. of Gate drivers	4. n	8. n	2.64 n	3.96 n	3. n	5.38 n	4. n
Semiconductor losses	=	highest	Lowest	high	Moderate	Moderate	Low
Fault handling	No	Yes	No	Yes	Yes	Yes	Yes
Control complexity	high	highest	low	low	lowest	low	lowest

Assuming generating the same number of output voltage levels of 2n+1 per leg of the MMC

The mixed cell-based proposed converter is capable of generating five voltage levels using a cell, hence this topology requires one-third times lesser cells concern to traditional symmetrical half-bridge (HB-SM) cells. An exhaustive scientific comparison among different existing traditional symmetrical cell topologies and novel asymmetrical cells is presented in Table 4. To achieve the same number of output voltage levels, the symmetrical half-bridge and full-bridge SMs require three times the number of SMs, concerned with binary GP-based SM, and four times the number of SMs concerned with ternary GP-based SM. If DC fault handling capability is a must, the asymmetric FB cells or mixed cell can be used. In a physical hardware model, additional components are like protection SCR and bypass switches for safety and maintenance. Also connecting cells requires high current-carrying busbars. As can be seen, the use of A-MMC reduces the requirements of such components as illustrated in Table 4. A lesser number of control switches requires a lesser number of gate drivers, which can reduce the overall size and capital cost of the HVDC system. It also increases its reliability, and compactness and reduces complexity. The higher device stress and unequal ratings of control switches are some of the limitations of A-MMC. Overall, the A-MMC proves to be a promising option for a modular structure to be used in future HVDC applications. The A-MMC topology provides some essential advantages which make it a viable candidate, to be considered as an alternative to the conventional MMC.

6. CONCLUSION

DC-side fault blocking capability with reducing component count in MMC is a major challenge. In this article, the asymmetrical mixed-cell-based A-MMC has been projected as a converter with reduced component count and improved DC fault-blocking capability. To control its operation, a novel voltage balancing (VB) algorithm and hybrid pulse width modulation has been illustrated and successfully verified with asymmetrically charged capacitors of the cell. Through simulations in MATLAB/Simulink, the hybrid PWM-driven operation of A-MMC and the effectiveness of its voltage balancing blocks were confirmed. A comparative study of proposed topology and traditional topologies was done

and the proposed A-MMC performed superior, in terms of efficiency and improved DC fault blocking capability. An analytical circuit component count comparison among different MMC topologies was also done and the A-MMC was found far superior. The performance of A-MMC was found better for other parameters like capacitor voltage ripple, circulating current, output current, and voltage THD. From that, it is said that the A-MMCs will be a viable alternative to the MMCs in future HVDC implementation having a more compact and efficient system.

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